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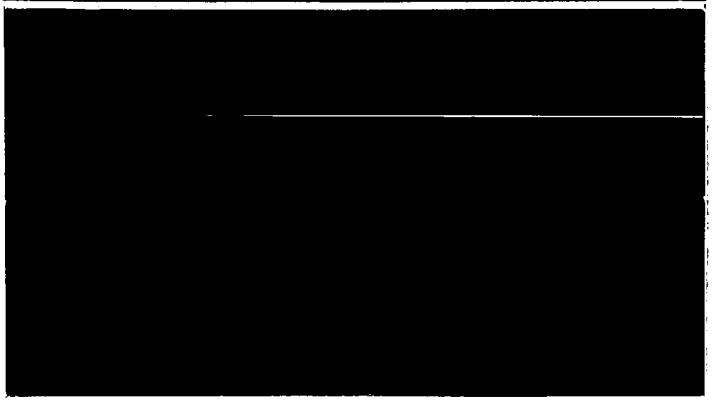
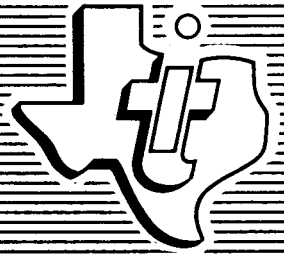




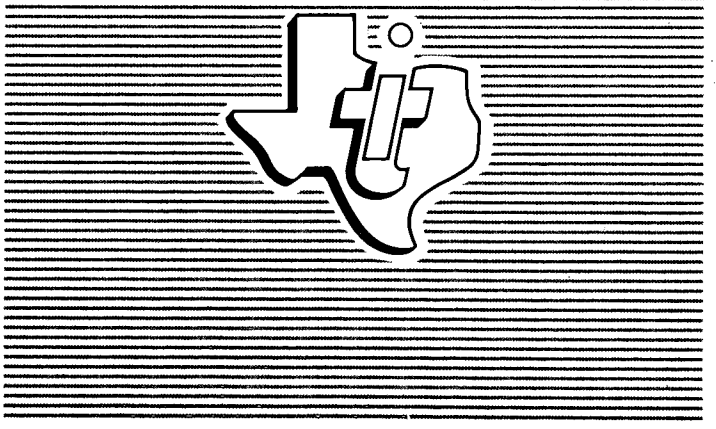
TEXAS INSTRUMENTS
INCORPORATED

FINAL REPORT
AIRBORNE ELECTRONICALLY STEERABLE PHASED ARRAY

July 1972

Prepared for

NATIONAL AERONAUTICS
AND SPACE ADMINISTRATION
Marshall Space Flight Center
Huntsville, Alabama



Equipment Group
U1-977580-F
Contract No. NAS8-25847

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FOREWORD

This report contains the results of a 12-month critical hardware development of an Airborne Electronically Steerable Phased Array System, under Contract NAS8-25847, sponsored by the Astrionics Division of NASA Marshall Space Flight Center are described in this report. Dane O. Lowrey is the cognizant engineer and Robert W. Shankle is the contracting officer.

The work was performed at the Texas Instruments Equipment Group Research and Development Laboratory under Glenn Gaustad, Antenna and Microwave Systems department manager. Project engineer for the first 7 months was Sam B. Roberts. Principal contributors included V. Ward McClure (Antenna and Manifold) and Wayne Harrison (Module) assisted by Chris O. Hemni, Jim Nix, Charles Moore, Ronald Allison, and Jack Reynolds. Project engineer is Allen S. Jones.

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June 1972

FINAL REPORT
AIRBORNE ELECTRONICALLY STEERABLE-PHASED ARRAY

Reference: NASA Marshall Space Flight Center Contract No. NAS8-25847

SECTION I

INTRODUCTION AND DESCRIPTION OF CONTRACTUAL WORK REQUIREMENT

This report contains results of the second phase of the Airborne Electronically Steerable Phased Array (AESPA) program sponsored by the Astrionics Division of NASA Marshall Space Flight Center under Contract Number NAS8-25847. The first phase of this program was a 9-month design study leading to specifications for a 128-active-element, unified S-band, phased array terminal, having high reliability over a 5-year time period, low weight comparable to, or less than a conventional low-gain, high-power system. This specification was contained in the first phase report.* The second, or current phase being reported discusses the development of the critical hardware described in the first phase report including the 128-element array, the RF manifold, and the module. These are discussed in Section III of this report. Recommendations for future work are included in Section IV as a consequence of the results summarized in Section II.

The purpose of this program is three-fold.

- To develop a highly reliable solid-state S-band communication terminal system applicable to low- and high-altitude, reusable and permanently-placed satellites.
- To provide high-gain electronic beam steering without incurring a weight penalty.
- To develop a highly efficient modular antenna concept applicable to moderate apertures driven by fully duplexed, electronic transceiver modules.

The original specifications contained in RFQ 1-0-40-93877 are summarized in Table 1-1. The objective of this second phase is a continuation of the design and development of an airborne electronically steerable phased array capable of simultaneous and separate transmission and reception of radio frequency signals at S-band frequencies. The design goals of this phase were the development of three major areas of interest required for the final prototype model. These areas are the construction and testing of the low-weight, full-scale 128-element array of antenna

*A Preliminary Design of An Airborne Electronically Steerable Phased Array, U1-116817-F, 29 January 1971, Texas Instruments Incorporated.

TABLE 1-1. PERFORMANCE SPECIFICATIONS

Scan angle: 60 degrees from broadside (max)
Scan increments: <2.5 degrees
Transmit frequency: 2282.5 MHz
Transmit gain: 20 dB at max scan
Frequency stability: ±0.003 percent
Input impedance: 50 ±3 ohms
Power output: >25 watts at 2282.5 MHz
Polarization: Right-hand circular (RHCP)
Antenna efficiency: 60 percent or greater (at f_T)
Beamwidth: 10 degrees (60 degrees from broadside)
Sidelobes: 12 dB below mainlobe at max scan
Grating lobe: Suppressed below max scan
Bandwidth (XMTR): 30 MHz (min); 60 MHz (max)
VSWR: 1.5 max at any scan angle
Modulation (XMTR): FM
Modulation input impedance: 10,000 Ω (0 < f < 200 kHz)
Modulation distortion: down 35 and 45 dB for 2nd and 3rd harmonics, respectively, at 300 to 500 MHz with peak deviation of 50 kHz
Intermodulation distortion: down 40 dB
Deviation sensitivity: 200 ±10 kHz/rms volt
Deviation linearity: ±1 percent, Δ < 200 kHz; ±2 percent, Δ < 500 kHz
Carrier deviation: ±500 kHz
Frequency response (XMTR): ±1.5 dB with respect to 50 kHz, 0 < f < 500 kHz
Temperature cycling: −20° to 85°C
Acceleration: 50 g in three orthogonal planes
Shock: Half sinewave, 50 g for 11 ±1 μs
Altitude: 9 months, p = 10^{-7} mm Hg
Moisture resistance: relative humidity 95 percent with 15° < T < 70°C
Thermal vacuum: 50M 71810
Sinewave vibration: 10 to 2000 Hz, 20 g peak in three orthogonal planes
Random motion: 25 g for 5 minutes in each of three orthogonal planes
Acoustical noise: 50M 71810
RFI: MIL-I-6181D
Incidental FM: 8 kHz max
Incidental AM: 5 percent max
Protection: Capable of open circuit, short circuit or ±28 volts applied to modulation input
Receive frequency: 2101.8 MHz
RCVR bandwidth: min 30 MHz max 60 MHz
Polarization: RHCP
Receive Gain: 25 dB at max scan
Noise figure: 10 dB max
Output frequencies: IF (60 MHz) baseband, 2101.8 MHz
Output impedance: 50 ±3 Ω
Aperture: 225 elements (max)
Operational modes: self-focusing, pointing-logic controlled, hybrid
Prime power source: 28 ±4 volts (Z_o < 1 Ω)
Conversion efficiency (dc to RF) ⩾ 10 percent
Grounding: 10^7 Ω isolation
Polarity reversal (28 ν): no effect
Radius of curvature ∿ 300 cm
Mounting: Flush mount
Covering: Adequate for reentry heating
Size: Thickness not to exceed 6 inches
Weight: not to exceed 25 pounds
Construction: MIC
Reliability: MTBF, 50,000 hours, 30,000 hours continuous operation
Thermal shock: 20° to 85°C

elements, the development of the RF manifold feed system, and the construction and testing of a working module containing diplexer and transmit and receive circuits.

This phase consisted of the following tasks which utilized preliminary design results attained during the first phase.

1. Finalize the element design, fabricate and test a full-scale 128-element array of antenna elements which meet electrical specifications and utilize construction techniques that provide maximum ease of array assembly.
2. Fabricate and assemble a manifold subsection as a check for fabrication ease and electrical characteristics.
3. Develop and fabricate a full-size array manifold feeding system, following the satisfactory completion of the manifold subsection.
4. Perform testing on the assembled 128-element array, manifold feed system and lightweight support plate.
5. Utilize element pattern and mutual coupling data by calculating and evaluating the array patterns and impedance versus scan angle. Measure broadside patterns and two or more beam-steered patterns by means of cables cut to the proper lengths to act as phase shifters.
6. Finalize the design and construct a breadboard module complete with transmit and receive circuits and diplexer.
7. Perform testing and evaluation of the module to determine the environmental limitations on the module contents. Testing shall include measurements such as gains, efficiencies, bandwidths, thermal properties and noise figures over the temperature range of interest. Perform a refined reliability analysis of the module, utilizing the data obtained.

SECTION II
SUMMARY OF ACCOMPLISHMENTS

During the second phase of the program, effort was concentrated on achieving the electrical parameters of the array terminal; that is, equivalent isotropic radiated power (EIRP) and gain-to-noise temperature ratio (G/T). As discussed in the first phase report, the efficiency of this concept allowed a lower noise temperature to be employed than originally specified by NASA, resulting in a lower gain antenna. The EIRP was easily achieved through use of 1-watt transmitter elements. To demonstrate that this gain may be achieved with a lightweight, direct radiating antenna, the 128 active-element antenna shown in Figure 2-1 was constructed. This antenna weighed 10.25 pounds including structure. Each of the 128 active array elements are driven by electronic modules. The prototype aluminum module case, weighing 0.27 pound has two levels and is shown in Figure 2-2. The transmitter level shown at the left of the figure is at the rear of the array in close proximity to the thermal control system. The receiver level is next to the distribution and combination manifolds. The physical signal flow through the array is shown in Figure 2-3. An exploded view of the array concept is shown in Figure 2-4. The RF transmit distribution manifold shown in Figure 2-5 weighed 6.48 pounds, including connectors.

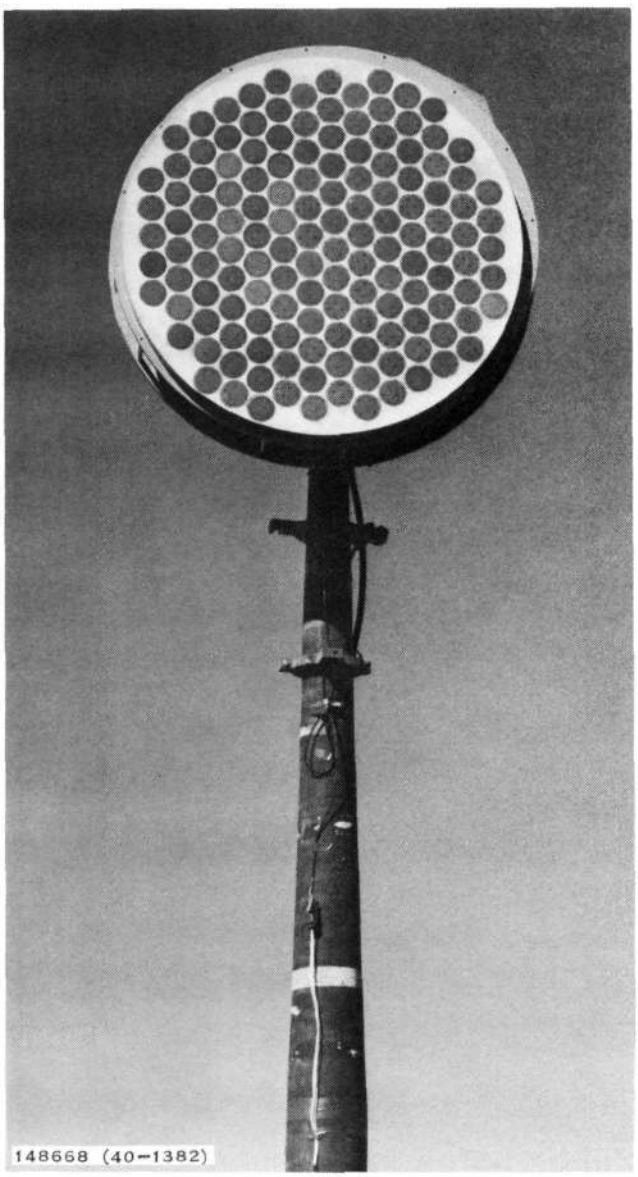


Figure 2-1. 128-Active-Element Antenna

Table 2-1 lists the technical achievements of this critical hardware development phase. In the original Texas Instruments proposal, certain parameters such as noise figure were projected into the 1974 time-frame of interest and were not expected to be achieved in this phase. A noise figure approaching the 5-dB design goal was achieved. Transistors recently were announced which made this goal achievable and are included in recommended future work. Additional noise figure reduction can be obtained by improving the diplexer filter and transmitter noise filter performance. Improved power transistors have been announced which will improve transmit efficiency with better thermal performance and reliability. The prototype electronics module case constructed in this phase was aluminum, as opposed to an aluminum/beryllium module originally proposed, to

TABLE 2-1. AESPA II TECHNICAL ACHIEVEMENTS

Subsystem Performance	Value
Antenna (2282 MHz)	
Boresight gain (dB)	23.9
60-degree scan gain (dB)	20.3
Boresight axial ratio (dB)	0.3
60-degree scan axial ratio (dB)	2.0
Weight (pounds)	6.48
Boresight sidelobe level (dB)	19.5
60-degree scan sidelobe level (dB)	9.0
Module	
Noise figure (dB)	6.0
Receive gain (dB)	24
Diplexer isolation (dB)	35
Peak phase shifter phase error (degrees)	10
RMS phase shifter phase error (degrees)	5.2
Phase shifter amplitude error (dB)	0.5
Phase linearity (degrees)	5
Power output (dBW)	0.5
Transmit gain (dB)	19.0
Transmit efficiency (percent)	25
Weight (pounds)	0.275
Transmit Manifold (128-Element)	
Peak phase error (degrees)	±5.25
Peak amplitude variation (dB)	±0.6
Peak output VSWR (Ratio:1)	1.65
Loss (dB)	3.2
Weight (pounds)	6.48

lower the cost of the feasibility demonstration. Even considering this material substitution, module weight requires further reduction. Thus, the major improvement in future engineering phases is in the area of weight reduction.

The construction of the 128-element spiral array has shown the feasibility of the array approach for space telecommunication. Completion of the feasibility demonstration by filling the array with electronic modules and operating it with a modulator and receiver will be an important milestone in the demonstration of the total system concept.

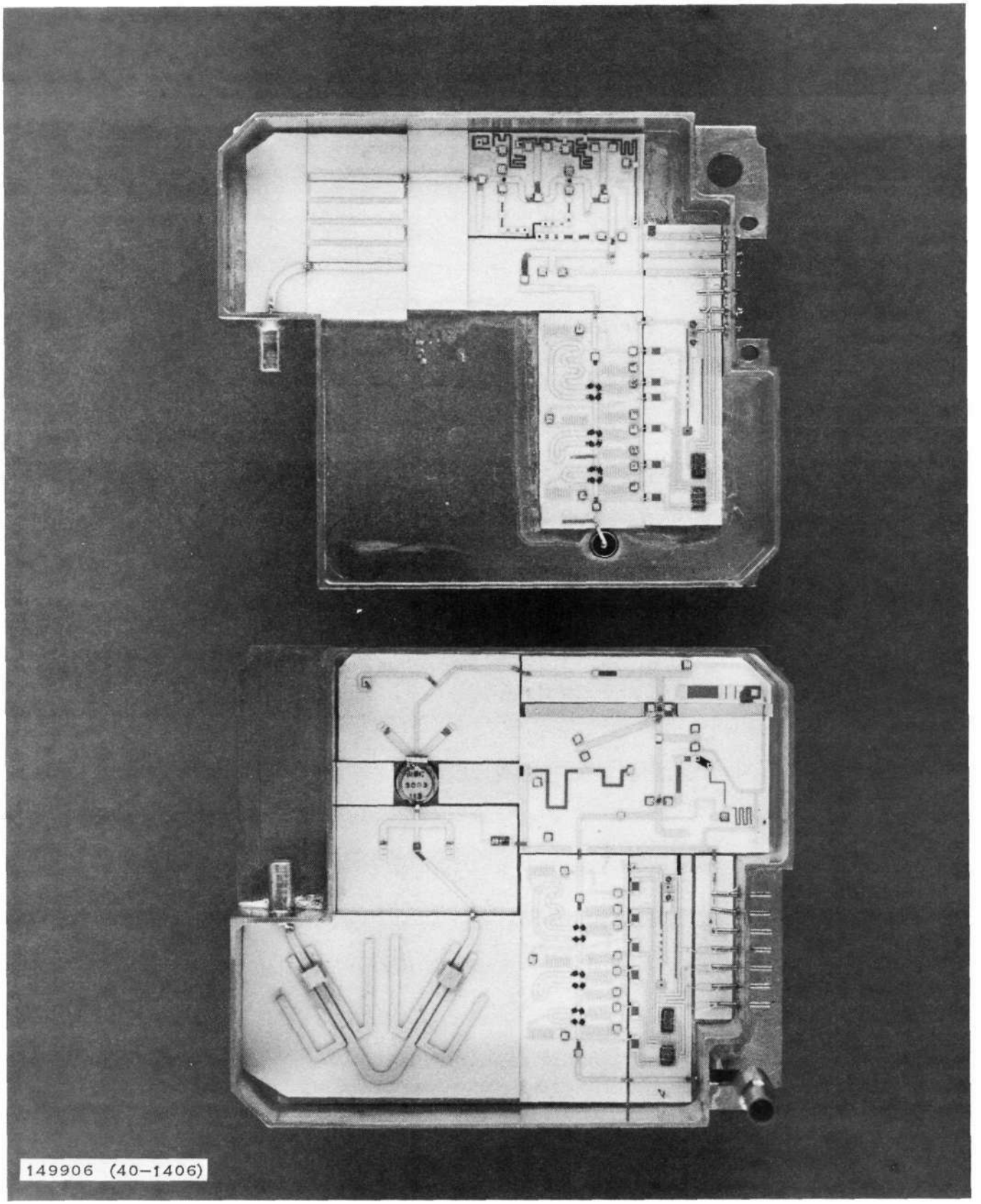


Figure 2-2. Aluminum Prototype Module

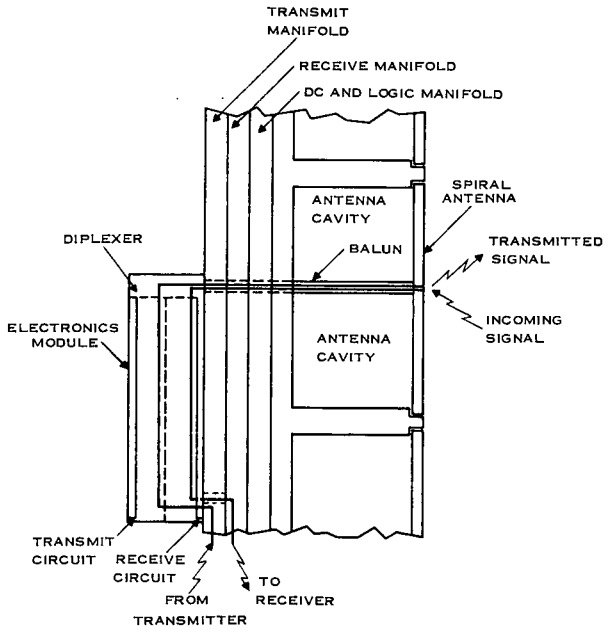


Figure 2-3. Array Signal Flow

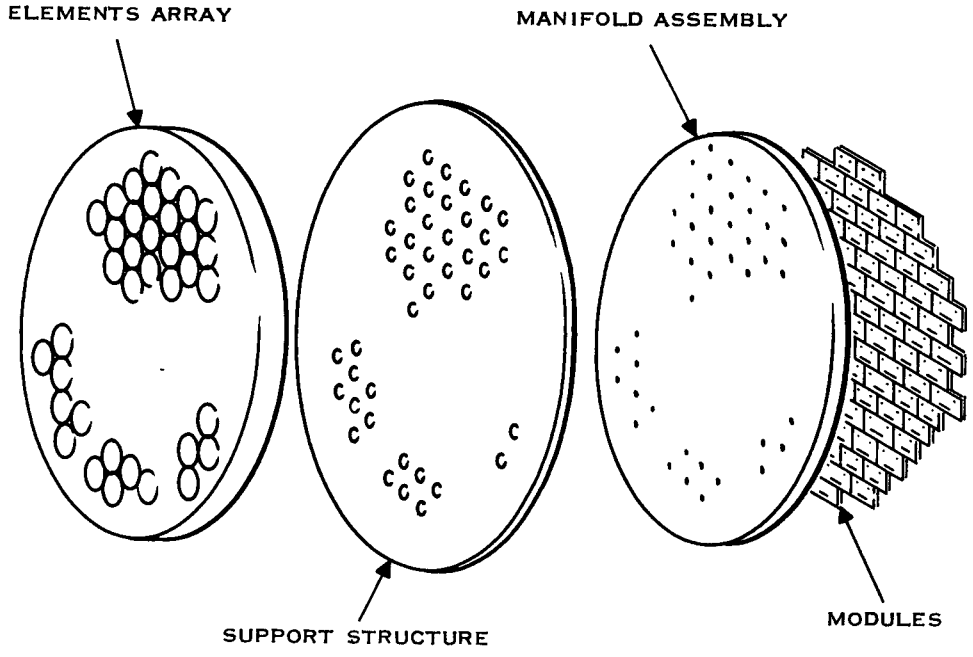


Figure 2-4. Array Assembly for Airborne Electronically Steered Phased Array

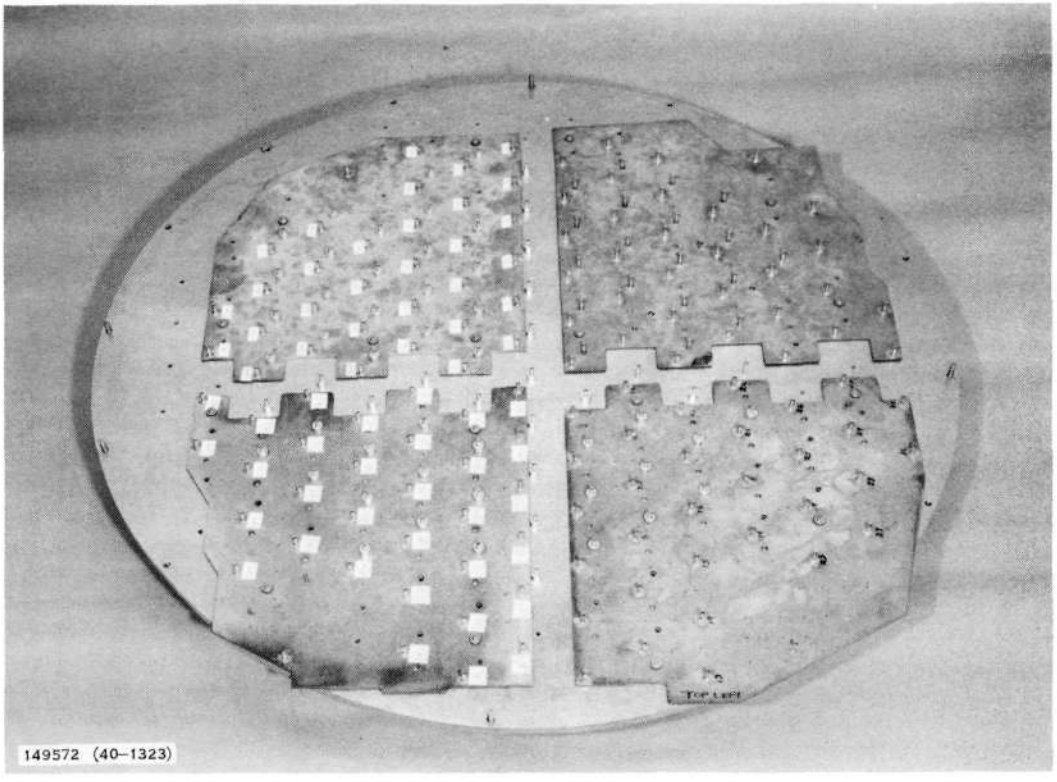


Figure 2-5. RF Transmit Distribution Manifold

SECTION III

ARRAY, RF TRANSMIT MANIFOLD AND MODULE DEVELOPMENT

A. Antenna Development

The AESPA antenna consists of 140 individual archimedes spiral radiating elements; of these, 128 are active. The elements are bonded to a closed-cell, plastic-foam cavity structure. A thin layer of conductive silver paint is applied to the foam cavity resulting in electrical performance comparable to that obtained with a much heavier metallic cavity structure. The combined weight of the antenna cavity and support panel is 10.25 pounds. In the subsections which follow, the various design approaches pursued in the development of the antenna element, antenna feed balun, and foam cavity structure are discussed.

1. Spiral Radiating Element

Two types of two-filament spiral antennas were investigated for use in the AESPA array. These were the equiangular, or log spiral, and the archimedes spiral. Gain, axial ratio, and radiation pattern beamwidths were compared for both types, when fed with the same type feed baluns.

The beamwidth, gain, and axial ratio of the planar equiangular spiral is dependent on the wrap angle of the spiral filaments. Geometrically, tightly-wrapped spirals with wrap angles approaching 90 degrees have more filament turns for a specified antenna diameter. Using the IBM-360 computer linked with a Gerber photoplotter, artwork for photoetching equiangular spirals with 70-degree, 75-degree, 80-degree, and 85-degree wrap angles was generated. Radiation patterns were obtained for each of the spiral geometries over a 2.0- to 2.4-GHz frequency range. These radiation patterns were taken on the center element in a 13-element prototype array (Figure 3-1). The 13-element array was constructed with plastic foam cavities which were coated with a conductive metallic silver paint. The construction techniques employed in fabricating the 13-element antenna served to refine the processes used in the complete 128-element antenna array as well as to provide a good electrical model for radiation pattern testing. The best performance was obtained with the 85-degree wrap-angle equiangular spiral. Radiation patterns for the 85-degree spiral are shown in Figure 3-2A. These radiation patterns were taken with a rotating, linearly-polarized source antenna. This method provides a simultaneous measure of the axial ratio of the antenna being tested, in addition to the other radiation pattern parameters.

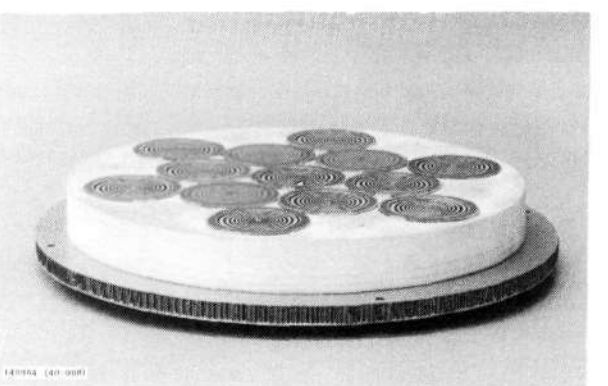


Figure 3-1. 13-Element Prototype Array

Since the AESPA bandwidth is narrow compared to the operating capability of the equiangular spiral, the typically narrower band archimedes spiral was examined in an effort to

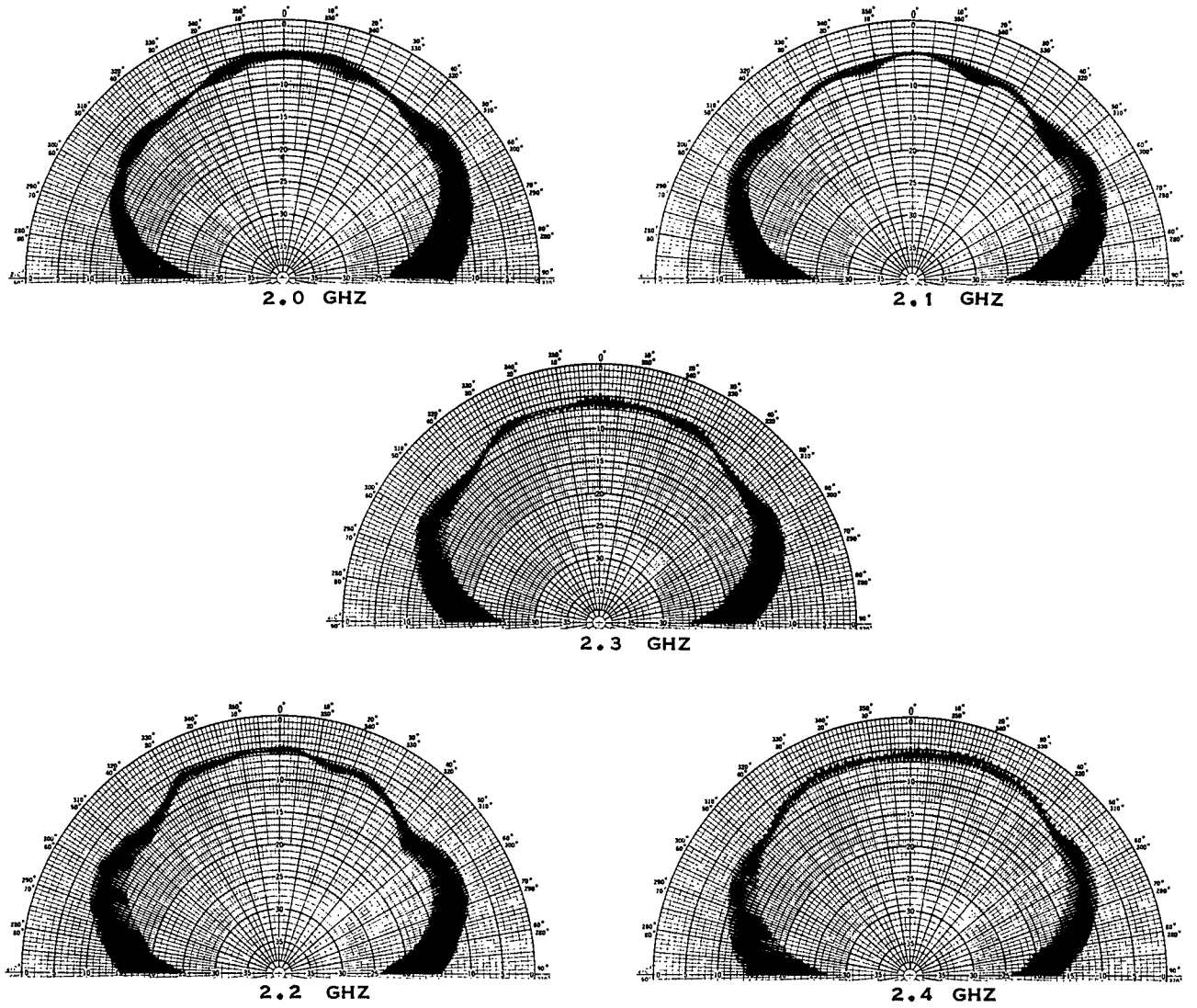


Figure 3-2A. Measured Element Patterns (Equiangular Spiral)

increase the element gain over the 2.1- to 2.3-GHz band. Gerber photo-artwork was generated for a two-filament archimedes spiral 2.90 inches in diameter with 20 turns per filament. The feed attachments on this antenna specifically were designed to interface with the Wolf and Bauer printed circuit balun. Radiation pattern data obtained on the center spiral in the 13-element array compared favorably to the results obtained on the 85-degree equiangular spiral. These patterns are shown in Figure 3-2B. The measured gain of the archimedes spiral, with respect to a circularly polarized isotropic radiator, was 3.35 dB at 2.1 GHz and 4.76 dB at 2.3 GHz. This is comparable to the gain obtained with the 85-degree equiangular spiral. Contrary to expectations, no increase in gain was achieved with the archimedes spiral. However, since the arm widths of the archimedes spiral are wider in the feed-point region, soldering the printed circuit balun to the spiral arms was considerably easier using the archimedes spiral. This resulted in reduced fabrication time and reduced scrappage as a result of the copper spiral arms loosening from the

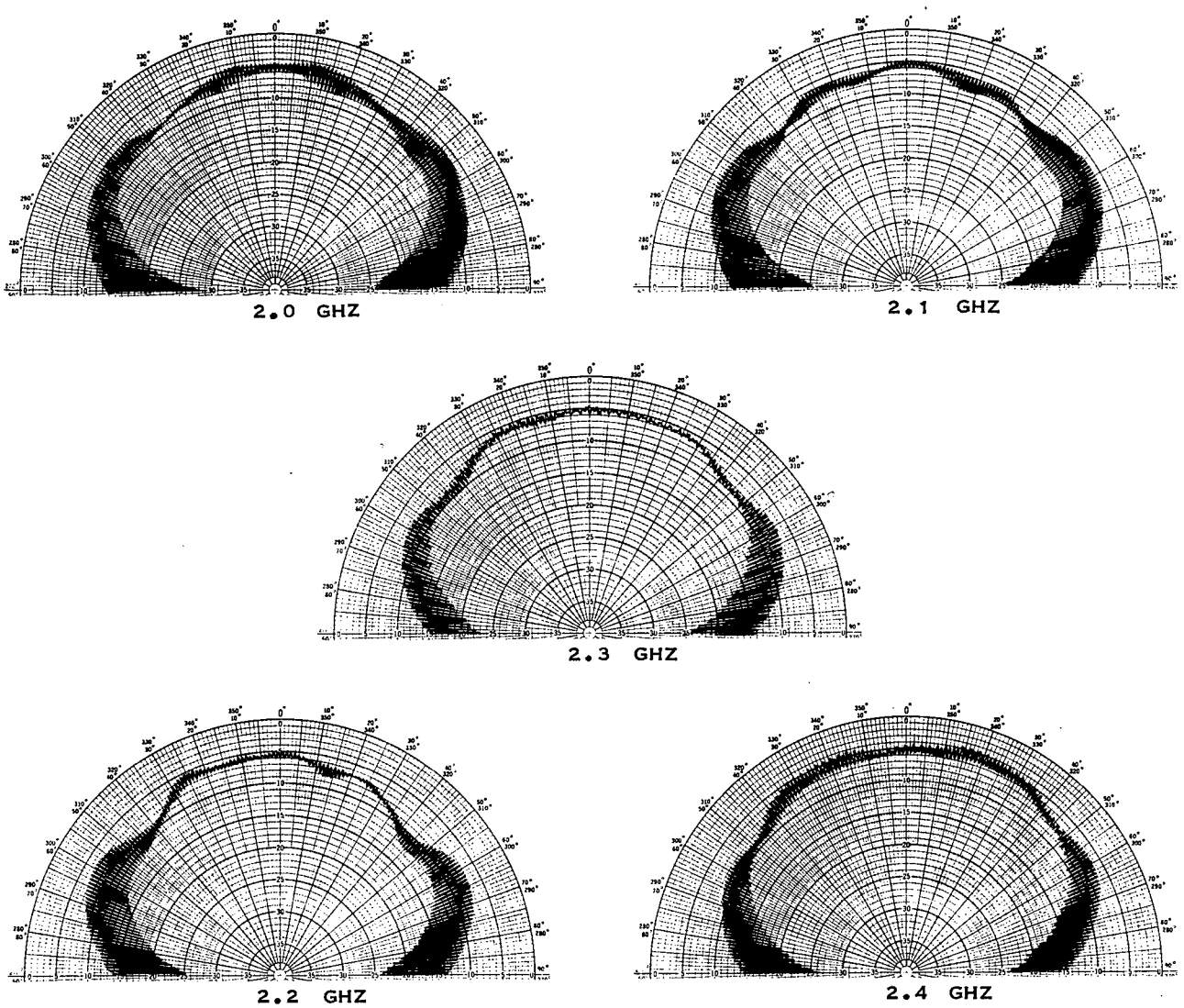


Figure 3-2B. Measured Element Patterns (Archimedes Spiral)

fiberglass substrate during the 400°F soldering operation. Figure 3-3 is a copy of the photomask used in photoetching the 140 spiral elements used in the AESPA antenna. Only 128 of these sprials are connected to the RF manifolds. The remaining 12 elements are resistively terminated inside the antenna cavities. These elements provide physical symmetry to the overall array ground plane surface. This improves the symmetry of the radiation patterns for off-axis steering angles.

2. Feed Balun Development

Three basic types of balun designs could be used to feed the AESPA spiral antenna elements. These are the tapered balun, the split-tube balun and the Wolf and Bauer balun. Figure 3-4 shows a schematic of each of the three types. The tapered balun and the split-tube

balun are constructed of brass and must be machined to achieve good repeatability from unit to unit. These balun designs were constructed during the development program and excellent electrical performance was obtained with each.

The Wolf and Bauer balun is a printed-circuit type which can be mass-produced by photoetching processes. Excellent reproducibility results. In addition, this balun when properly designed to match the antenna feed-point dimensions, can easily be soldered to the spiral antenna element.

Size, weight, ease of fabrication, as well as electrical performance are prime considerations in the overall AESPA design. The Wolf and Bauer design was superior in all of these categories, including electrical performance, over the AESPA operating band. Figure 3-5 shows the electrical performance of the finalized Wolf and Bauer feed balun when attached to the AESPA archimedes spiral element. This element was centrally located in the 128-element AESPA antenna. As shown in Figure 3-5, the VSWR is less than 1.30 over the AESPA frequency band and is well within the 1.50 VSWR design goal. Figure 3-6 is a photograph of the archimedes element with feed balun attached. These elements are bonded directly into the foam antenna cavity structure.

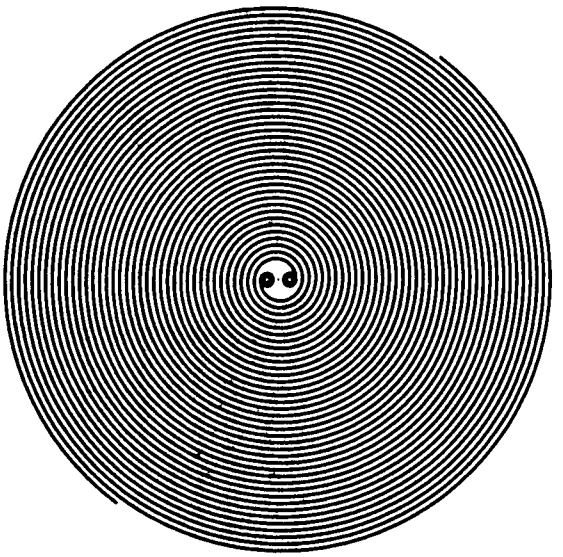


Figure 3-3. Photomask of Archimedes Spiral Antenna Pattern Photomask

3. Antenna and Support-Plate Fabrication

There are two basic structures in the AESPA antenna, the foam cavity structure and the honeycomb support plate.

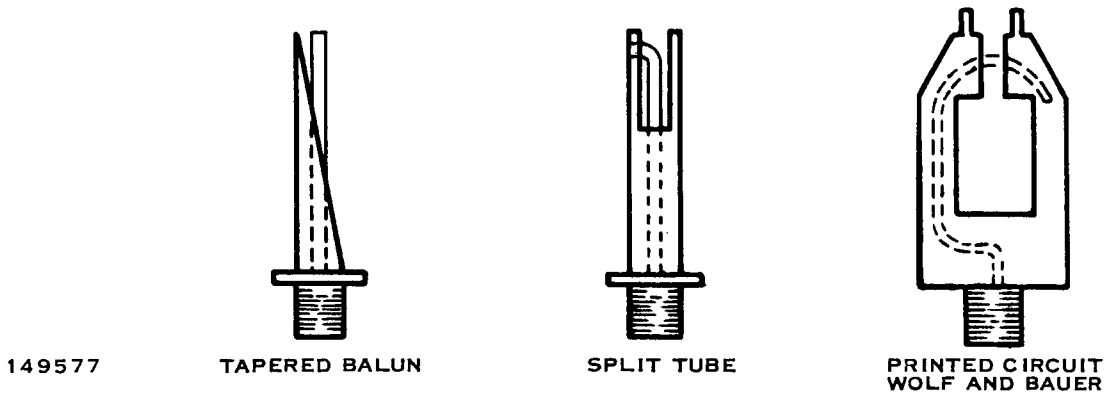


Figure 3-4. Balun Designs Investigated for Use on AESPA Spiral Antennas

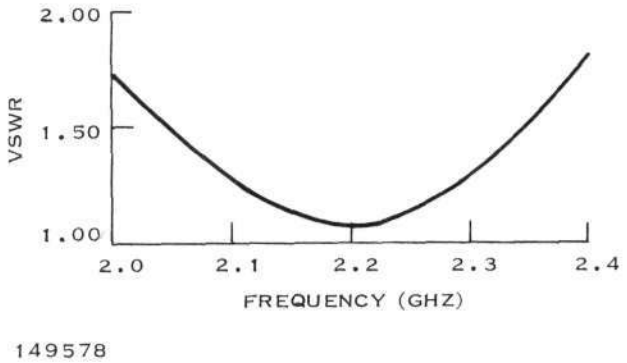


Figure 3-5. Measured VSWR of Centrally Located AESPA Spiral Element

To obtain maximum antenna gain and a nondirectional radiation pattern, the individual spiral antenna elements are mounted above a quarter-wavelength deep cavity. These cavities are 2.90 inches in diameter and 1.53 inches deep. The cavities are normally metal. Aluminum was initially considered. The use of aluminum cavities in the AESPA antenna design results in a weight of 47 pounds for the cavity structure, alone. Magnesium cavities were rejected because of expense and potential corrosion problems. The approach taken to achieve a lightweight structure with electrical performance equivalent to a metal cavity structure was the use of a conductive coated-plastic foam.

The foam chosen for the cavity structure is a closed-cell thermoset plastic having a density of 3.0 pounds per cubic foot. This foam has excellent chemical resistance, its moisture absorption is less than 0.1-percent, and it is capable of operating over the AESPA environmental requirement of -25° to $+85^{\circ}$C. The measured electrical performance of the foam cavity antenna is equivalent to that expected of a metal cavity. These results are presented in detail in a later section.

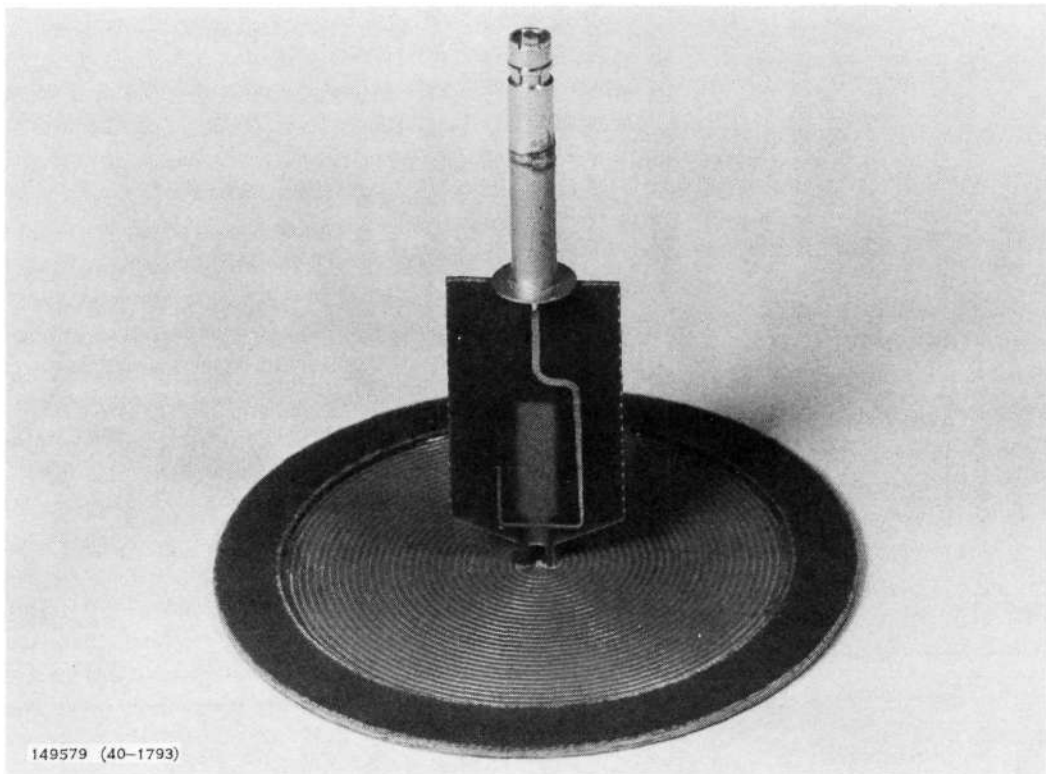


Figure 3-6. AESPA Antenna and Feed Balun Before Installation

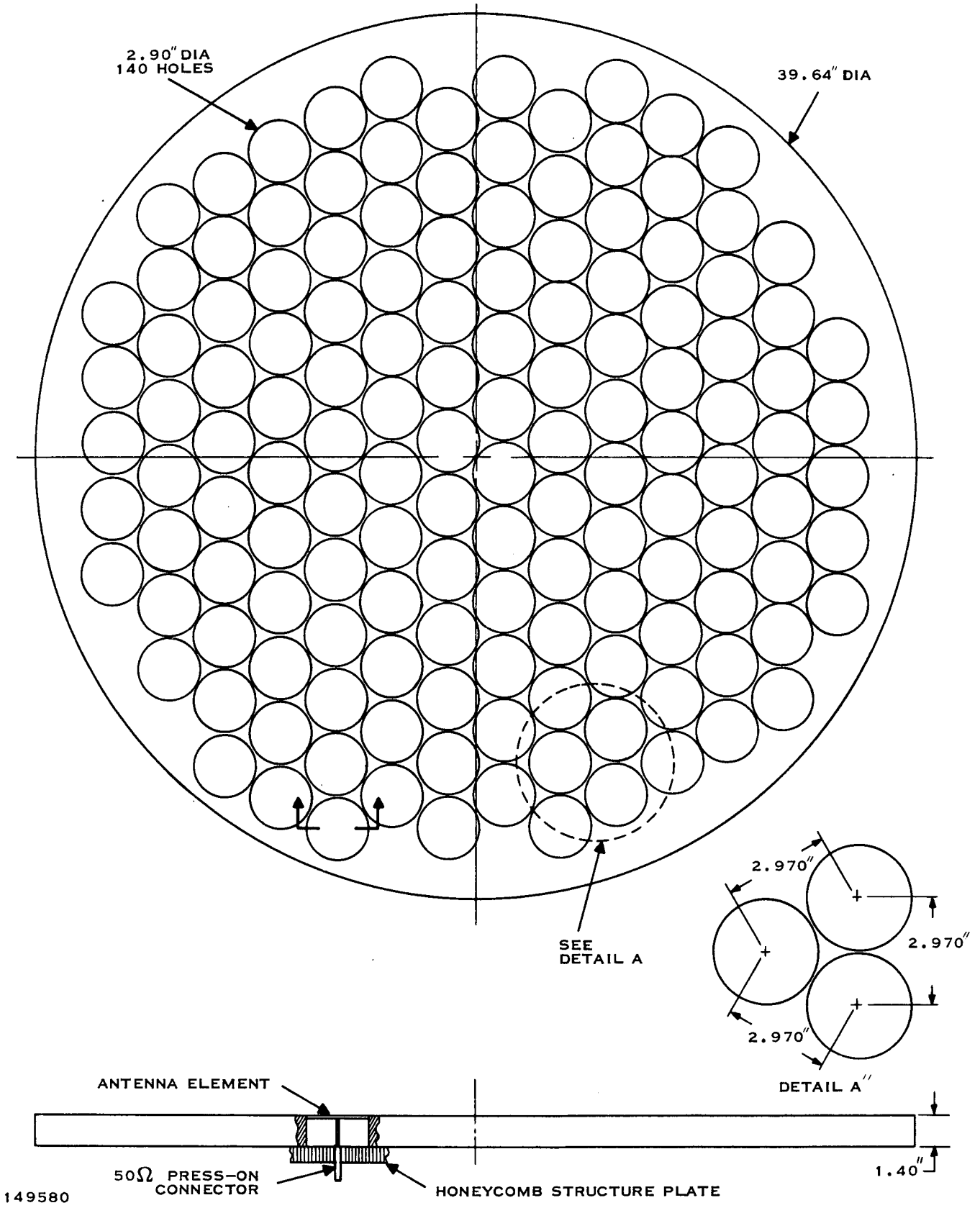


Figure 3-7. Layout of Foam Antenna Cavity and Honeycomb Support Structure

A tape-controlled milling machine was used in the antenna cavity construction. Approximately 8 hours were required to cut the 140 cavities. After fabrication, the foam cavity was bonded to the honeycomb support plate. This support plate is a sandwich structure consisting of a 0.5-inch aluminum honeycomb between two 0.012-inch aluminum skins. A high-temperature dry-film adhesive was used to bond the honeycomb and aluminum skins into a strong, lightweight support plate. This plate serves as the support structure for the entire AESPA antenna, manifolds, and microwave integrated circuit (MIC) modules.

The structural support plate is 1.0 inch larger in diameter than the antenna array. This provides a 0.5-inch wide space around the support plate for mounting the AESPA system to a frame on the spacecraft. Attachment holes are located around the circumference of the support plate in the 0.5-inch space.

The final step in the fabrication procedure is the application of the conductive silver coating to the cavity structure. This coating varies in thickness from 0.001 to 0.003 inch. Measured dc resistance of this coating was 0.2 ohms across the 39.64-inch array diameter.

Figure 3-7 shows a layout of the combined foam cavity and honeycomb support structure. Front and side views of the complete foam cavity structure are shown in Figures 3-8 and 3-9.

The AESPA array fabrication is completed by mounting the individual spiral antenna elements (Figure 3-7) into the foam cavity structure. These elements are secured with Epon 828

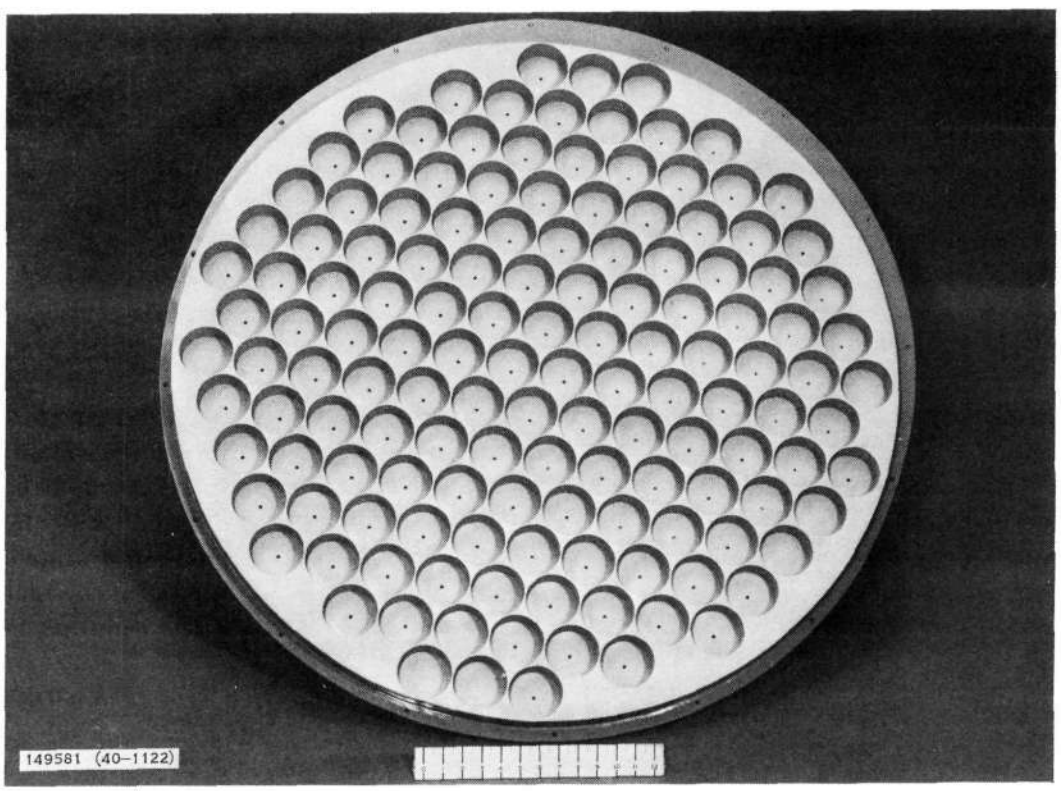


Figure 3-8. Foam Antenna Cavity Structure, Front View

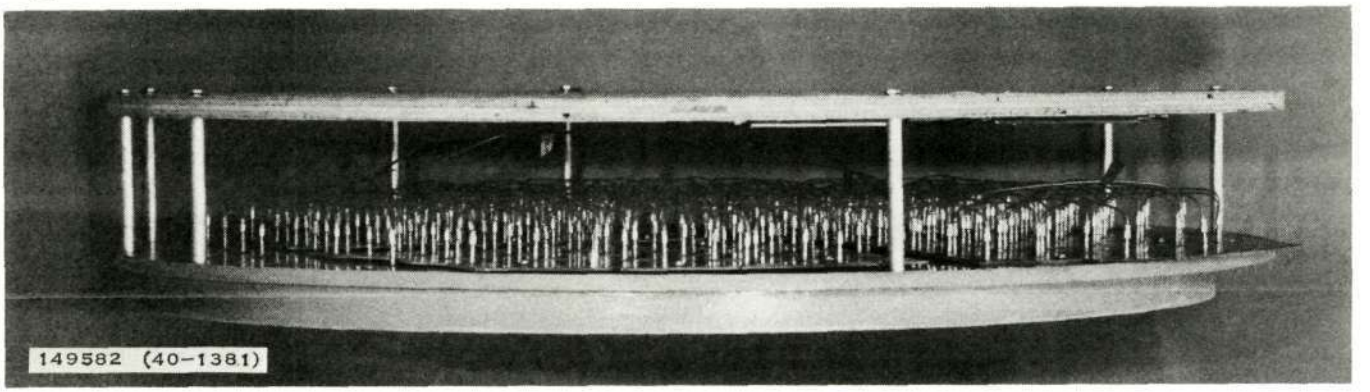


Figure 3-9. Showing Honeycomb Antenna Support Plate, Side View

epoxy and they are moisture-sealed with RTV adehesive sealant. A cross section of the foam antenna cavity with spiral element is shown in Figure 3-10.

4. Antenna Evaluation

The performance of the complete 128-element AESPA antenna and transmit manifold was evaluated by means of radiation pattern, gain, and VSWR measurements.

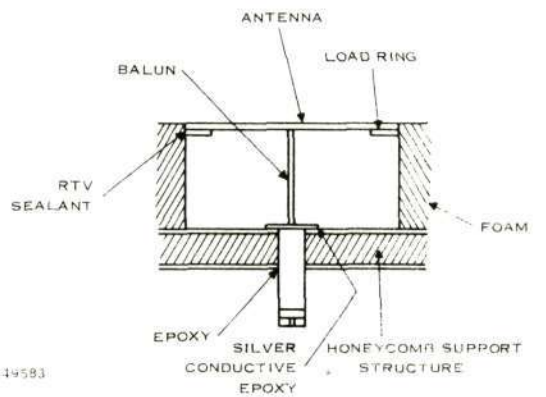


Figure 3-10. Spiral Cavity, Cross Section

The basic AESPA configuration was dictated by the requirement for easy accessibility to the MIC transmit/receive modules, allowing easy replacement of the MIC modules in a free space environment. To achieve this configuration, the antenna and manifold connections were positioned to match the connections on the MIC modules. Without the modules, auxiliary cables are required to interconnect the antenna and manifold for testing purposes. A total of 284 semiflexible, 0.086-inch diameter cables were fabricated for testing the completed array. The lengths of these cables were varied according to the required phased-shift increments between antenna elements for steering the antenna transmit beam to 0, 30, and 60 degrees in the azimuth plane. Figure 3-11 shows the AESPA coordinate system as it relates to the front face of the antenna. The azimuth, and elevation planes shown in the figure are those planes referred to in the data contained in this report.

To mount the antenna array on the antenna range positioner, a plywood range mount was constructed. This supporting structure was bolted to the antenna honeycomb support plate, using the attachment holes located around the outer circumference of the plate. The completed AESPA antenna, mounted at the Texas Instruments antenna range, is shown in Figure 3-12.

Radiation pattern testing consisted of measurement of the individual element patterns and overall azimuth and elevation array patterns. Azimuth radiation patterns were measured for

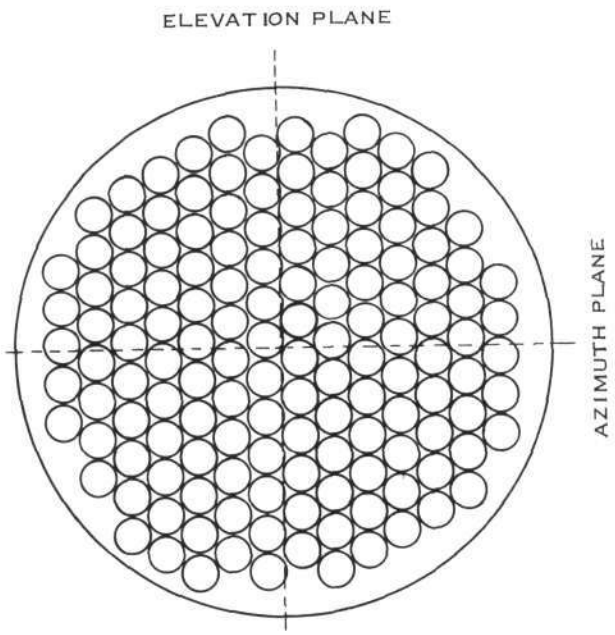


Figure 3-11. Radiation Pattern Data Coordinate System

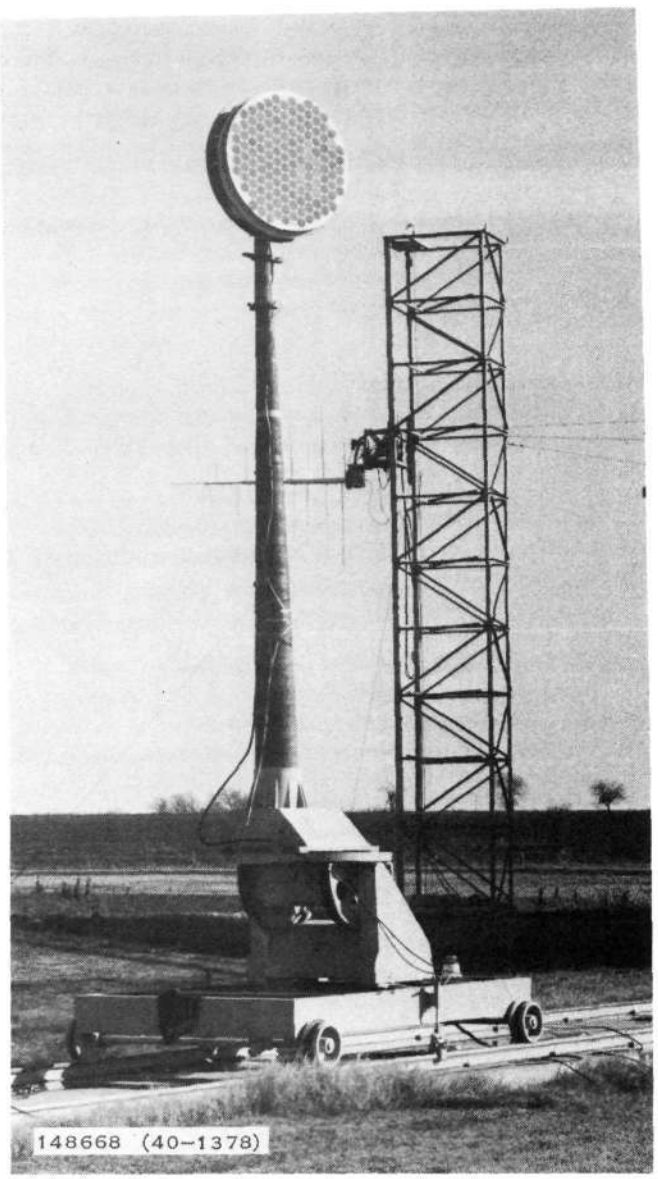
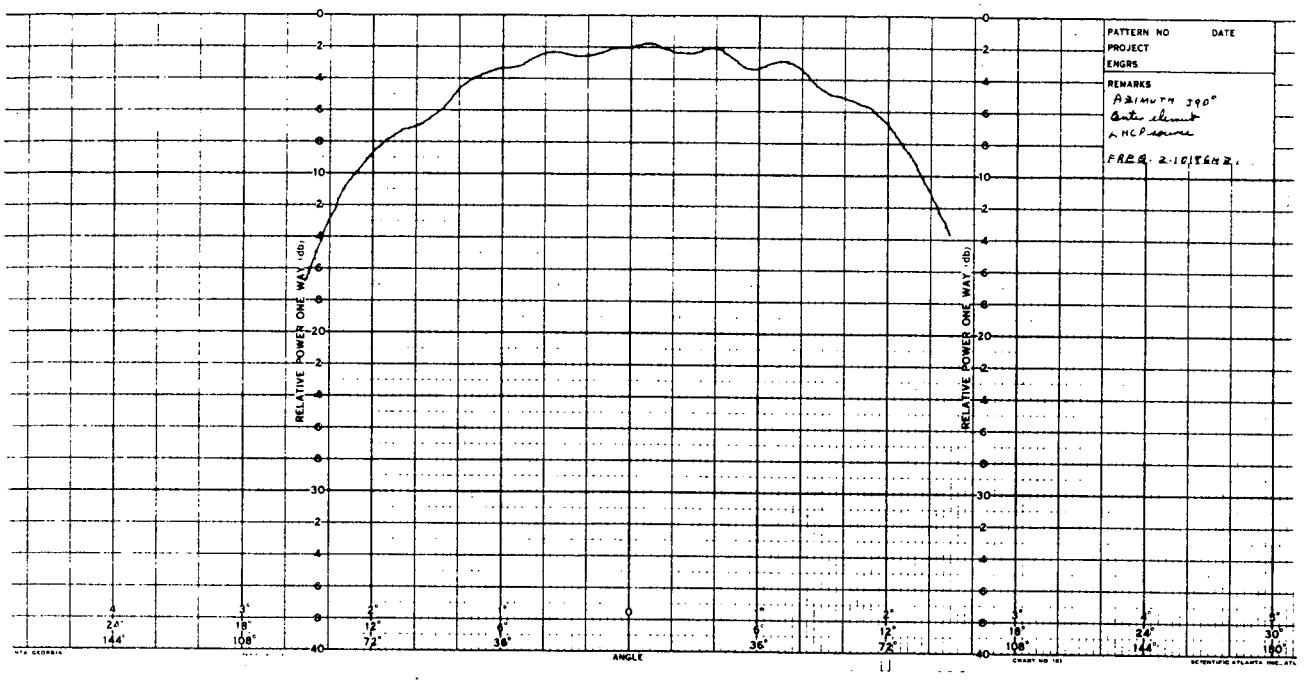


Figure 3-12. Complete AESPA Array Mounted on Texas Instruments Antenna Range

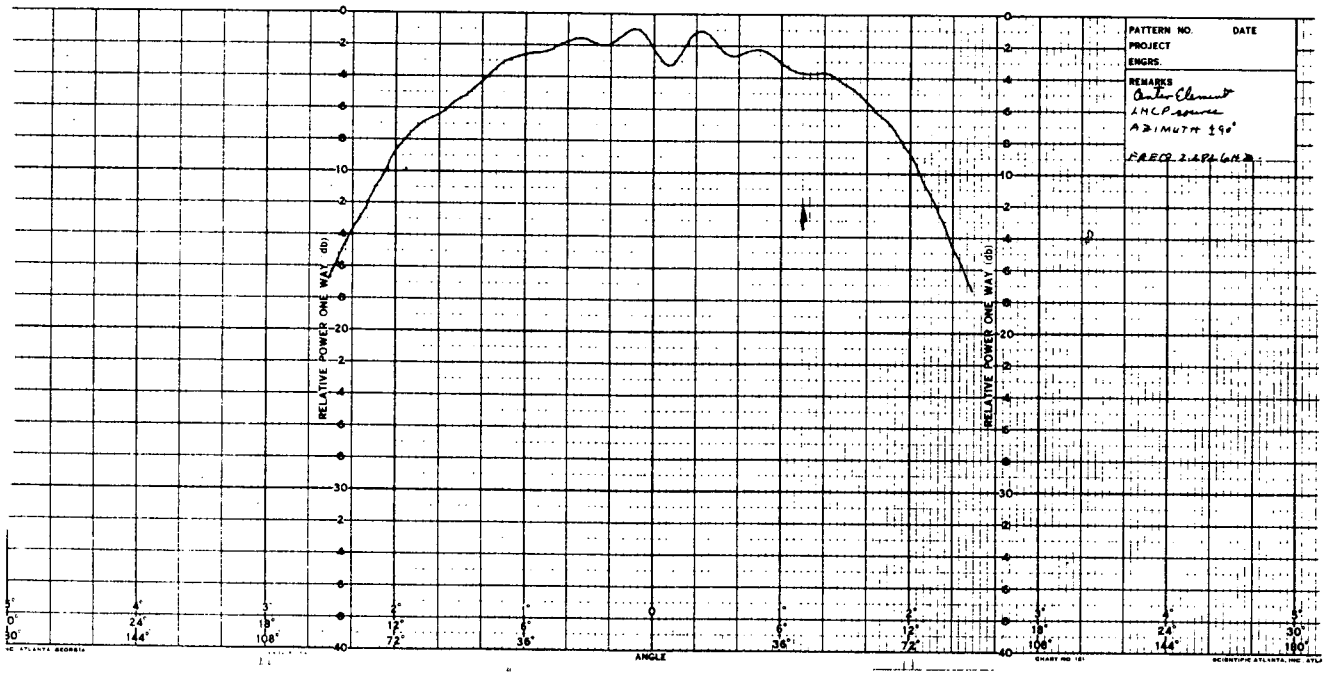
0-, 30-, and 60-degree scan angles. Fixed cable lengths were used to achieve the phase distribution across the face required for array steering to 30 and 60 degrees off broadside.

Figure 3-13 shows the radiation pattern of a centrally located spiral element. These patterns were taken at the AESPA transmit/receive frequencies of 2.101 and 2.282 GHz. Some variation in pattern amplitude occurs near the peak of the pattern. This variation is the result of perturbations caused by the antenna ground-plane structure and mutual coupling between spiral elements. The worst case amplitude variation is at the transmit frequency where the maximum rate of amplitude change is 0.2 dB per degree. These changes in amplitude are not expected to degrade the quality of data which would be obtained in operational earth-to-satellite communication links. The four outputs from the transmit manifold were connected using 180-degree hybrid couplers. Using this connection, sum and difference radiation patterns were taken at the AESPA transmit frequency for 0-, 30-, and 60-degree scan angles. The measured radiation patterns are shown in Figure 3-14.

A comparison of the measured radiation patterns with the theoretical calculated patterns in the Phase I final report shows excellent and favorable agreement between theoretical



A. ELEMENT PATTERN AT RECEIVE FREQUENCY – 2.101 GHZ



B. ELEMENT PATTERN AT TRANSMIT FREQUENCY – 2.282 GHZ

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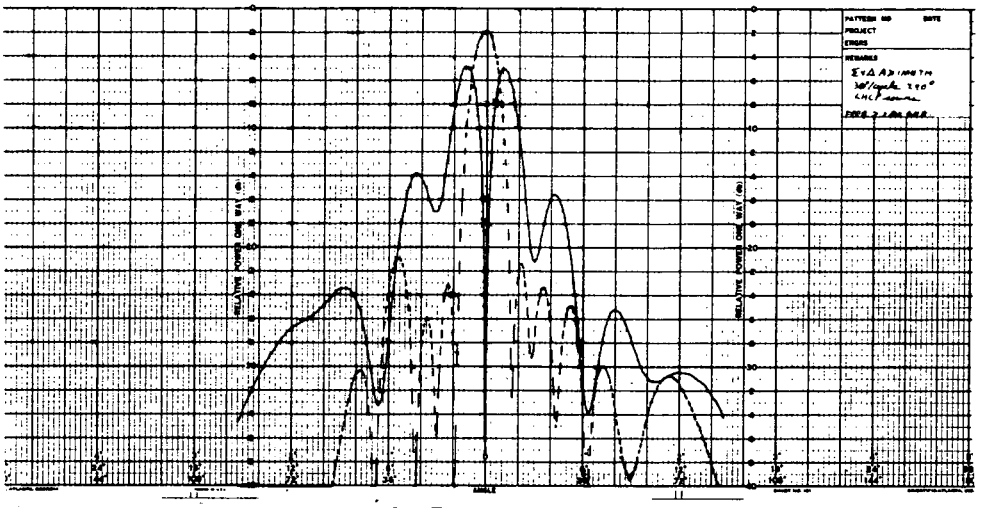
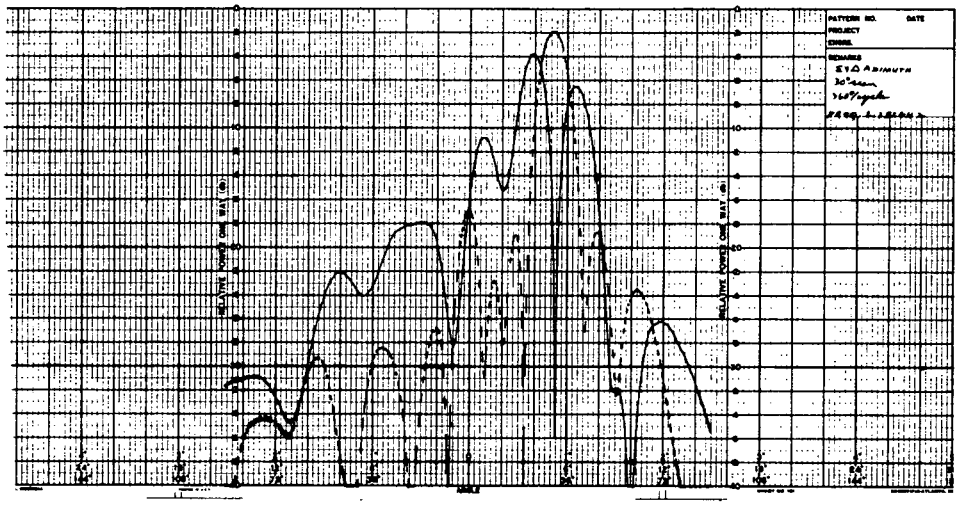
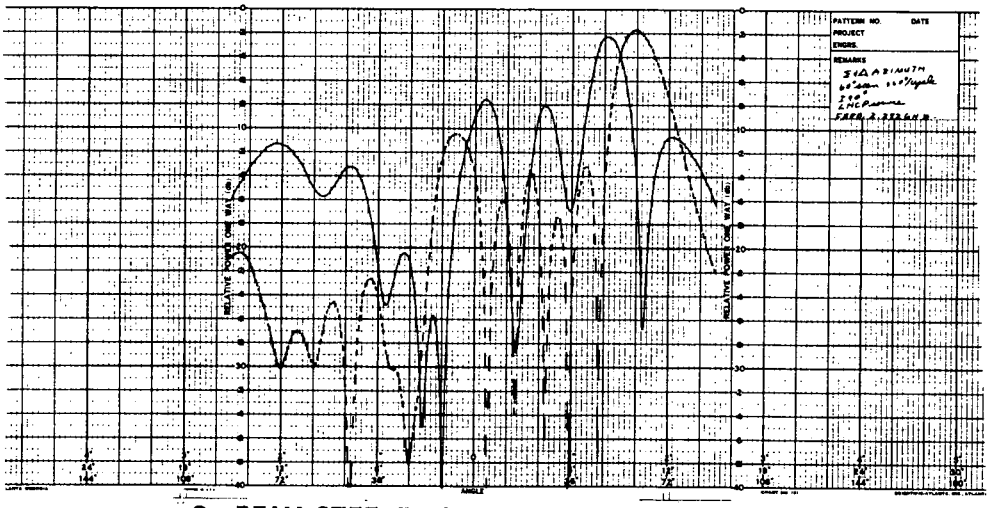
Figure 3-13. Measured Element Patterns of Centrally Located Special Antenna Element, Circularly Polarized Source Antenna



A. BROADSIDE



B. BEAM STEERED 30 DEGREES IN AZIMUTH



C. BEAM STEERED 60 DEGREES IN AZIMUTH

——— DIFFERENCE
– – – – – SUM

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Figure 3-14. Measured Azimuth Plane Sum and Difference Radiation Patterns of 128-Element Array, 2.97-Inch Grid

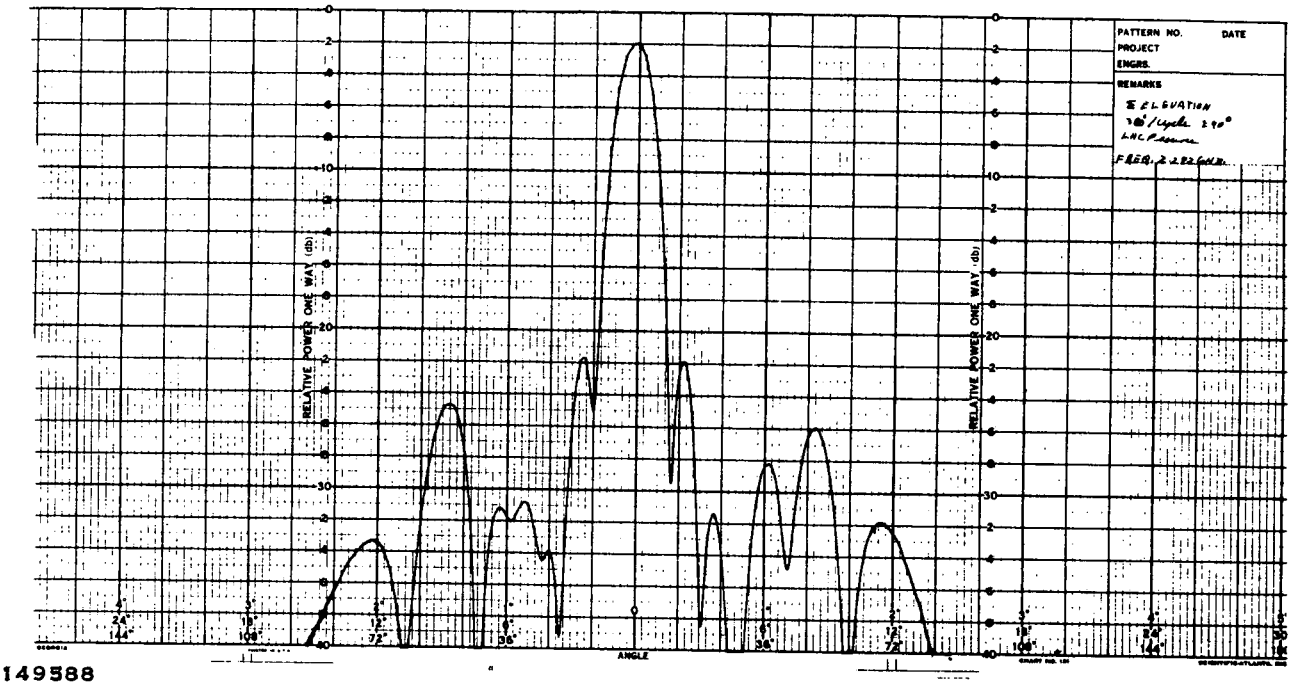

Figure 3-15. Measured Elevation Plane Radiation Pattern of 128-Element AESPA Array

and experimental results. The measured elevation radiation pattern of the complete 128-element array is shown in Figure 3-15. A complete summary of the radiation pattern measurements is contained in Figure 3-16.

Experimental measurements, were completed with the measurement of the array sum-channel input VSWR. A plot of the VSWR from 2.0 to 2.4 GHz (Figure 3-17) shows that a worst case VSWR of 1.40 was achieved with the AESPA transmit array. This is less than the AESPA performance goal of 1.50, established during the Phase I study.

The overall performance of the AESPA array exceeds the specified performance goals shown in Table 1-1 of the Phase I Final Report. In Figure 3-16, the gain of the complete 128-element array is shown to be 20.3 dB at the maximum scan angle of 60 degrees from broadside at the 2.282-GHz transmit frequency. This exceeds the AESPA goal by 0.3 dB.

B. RF Transmit Manifold

The AESPA RF transmit manifold is a 128-way corporate feed network. The basic function of the transmit manifold is to distribute the signals from the centrally located transmitter to each of the power amplifiers located in the MIC modules. After amplification, the signals travel directly into the 128 spiral antenna elements for transmission. This manifold operates at the 2.282-GHz transmit frequency.

SCAN ANGLE	GAIN WITH RESPECT TO CIRCULAR ISOTROPIC	NULL DEPTH WITH RESPECT TO SUM PATTERN	HPBW AZ	HPBW EL	Σ/Δ CROSSOVER BEAMWIDTH	MAXIMUM SIDELOBE LEVEL AZ	MAXIMUM SIDELOBE LEVEL EL
0°	23.9 DB	35 DB	9.0°	9.1°	10°	19.5 DB	20 DB
30°	23.4 DB	34 DB	10.0°	---	11°	14.0 DB	---
60°	20.3 DB	24 DB	16.0°	---	18°	9.0 DB	---

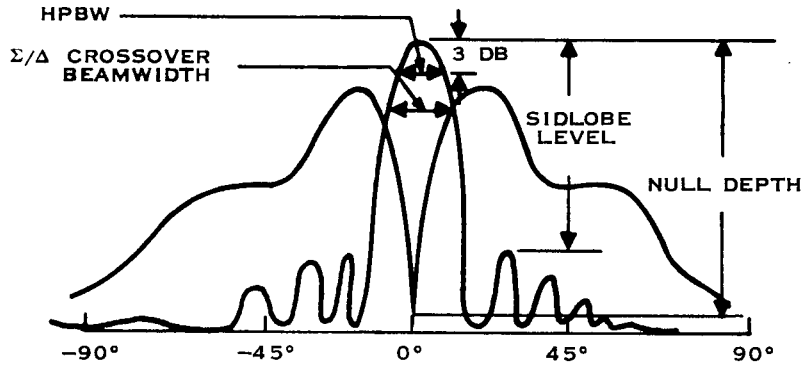

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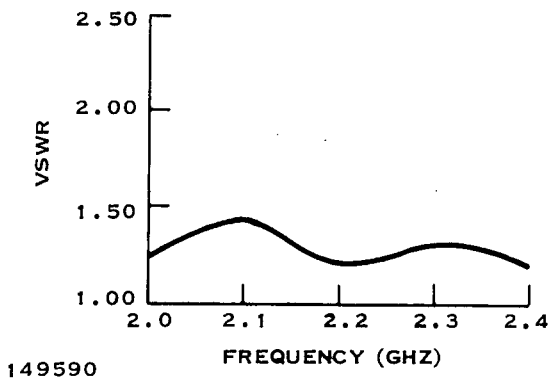
Figure 3-16. Performance Summary of AESPA at 2.282 GHz Transmit Frequency



149590

Figure 3-17. Sum Channel Input VSWR, All 128 Elements In Phase

The AESPA system contains a transmit manifold and a receive manifold. The transmit manifold purpose is to distribute power with equal phase and amplitude to each of the modules. The receive manifold combines coherently and weights the receive module outputs. These independently functioning units are planar in construction and are located physically between the foam antenna structure and the MIC modules. Strip transmission line is employed throughout both RF manifolds. During the AESPA Phase II study, the manifold design and development effort was restricted to the transmit manifold. Figure 3-18 is a block diagram.

1. Split-Tee Building Block

The basic building block in the transmit RF manifold is the split-tee divider. This design was chosen because of its ease of fabrication, excellent electrical performance and small size.

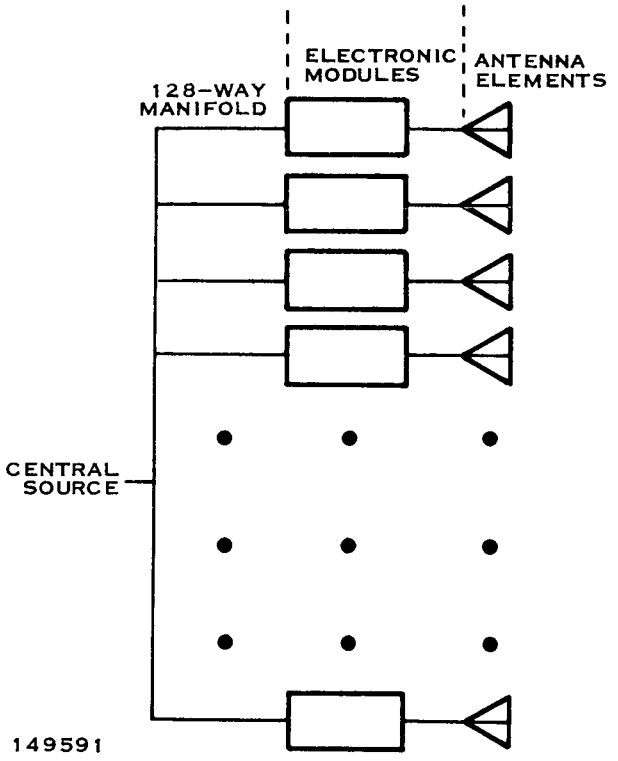


Figure 3-18. Electrical Block Diagram

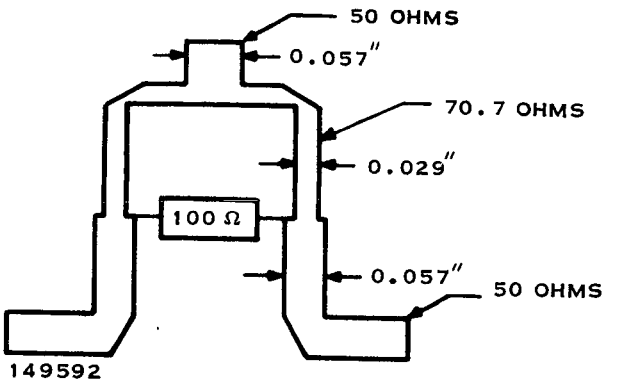


Figure 3-19. PPO Split-Tee Power Divider Dimensions

The objective for the overall manifold development was to design a basic building block and then to cascade basic building blocks into the complete 128-way corporate feed. The completed manifold is actually four separate 32-way manifolds which are combined through an external four-way power summing network.

The basic considerations which determine the design parameters of the split-tee power divider are the design frequency and the dielectric properties of the stripline material. Using these parameters, the basic design is calculated in two steps. The first calculation is that of the line width for 50 Ω and 70.7 Ω strip transmission line. Polyphenylene oxide (PPO) dielectric material was used in the AESPA manifold. This material was chosen primarily because of its light weight and its good electrical properties. In comparison to the more commonly used Teflon fiberglass composite materials, PPO is about one-half as heavy. Each layer of the PPO in the transmit manifold is 0.040 inch thick. Using a ground-plane spacing of 0.080 inch and a dielectric constant of 2.55, the line width of 50 Ω line was calculated to be 0.057 inch. The line width of the 70.7 Ω line is 0.029 inch. The second step is the calculation of the quarter-wave 70.7 Ω impedance transformer section length. This length is 0.850 inch for the AESPA transmit frequency. The resulting dimensions for the transmit split-tee design are shown in Figure 3-19.

The AESPA transmit manifold employs strip transmission-line circuitry throughout. Texas Instruments is well known for the manufacture and packaging of stripline circuitry. Highly advanced processes developed at Texas Instruments were utilized in the development of the AESPA manifold. Among these processes were the use of dielectric laminate material chemical bonding and the use of plated-through holes for RF grounding of the copper ground-plane surfaces. The input and output connections are subminiature press-on type RF connectors which are attached by direct soldering to the ground-plane surfaces. The bonded stripline package is significantly lighter than the conventional stripline design which uses heavy metal backing plates and mechanical methods such as screws rivets, or eyelets for RF grounding. The chemical bonding process results in a compact and lightweight manifold and gives a moisture-sealed unit.

TABLE 3-1. TYPICAL PERFORMANCE OF TRANSMIT MANIFOLD QUARTER-SECTION

Transmitter input VSWR	1.65
Module input VSWR	1.35
Insertion loss	3.20 dB
Amplitude unbalance	±0.60 dB
Phase unbalance	±5.25 degrees
Isolation	17 dB

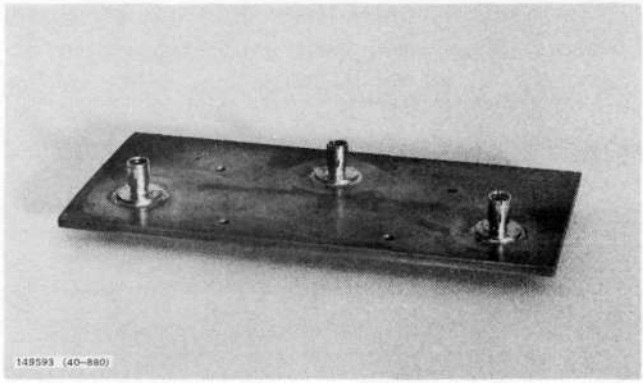


Figure 3-20. Transmit Manifold Split-Tee Building Blocks

Excellent electrical performance over the AESPA transmit band was obtained with the completed unit. Typical electrical performance of one of the manifold quarter-sections is shown in Table 3-1.

Since the overall electrical performance of the manifold depends primarily on the performance of the basic building block, the initial design effort was directed toward optimizing the split-tee design. Fabricating a single split-tee design provided a convenient test for optimizing the fabrication processes and the method of attaching press-on RF connectors. Figure 3-20 shows a prototype split-tee divider which has been chemically bonded and has the miniature RF connectors installed.

2. Quarter-Section Layout

The process for generating artwork for an entire 32-element quarter-section is explained in the following paragraphs.

The 32 manifold outputs are paired and combined with 16 split-tee dividers. The 16 dividers are then connected via 50 Ω line into eight power dividers. The eight split-tee dividers are combined into four, and so on until a single input is obtained. The complete manifold quarter-section contains 31 split-tee building blocks.

To optimize the performance of each of the quarter-sections as well as the overall manifold, it is critical that equal path lengths be maintained from the manifold input to each of the 32 outputs. This ensures that the output amplitudes will be identical and that equal phase outputs are maintained. When determining the path lengths of the interconnecting 50 Ω circuitry, it is important that the amplitude and phase perturbations caused by the stripline bends be accounted for.

The task of laying out the transmit manifold was compounded by the restriction that both the spiral antenna and receive manifold connections must pass through the transmit stripline circuitry. During the layout, extreme care was exercised to ensure that clearance was left to allow passage of these connections without interfering with the electrical performance of the transmit stripline circuitry.

The photomask for photoetching the manifold quarter-sections was made by cutting a Rubylith mask two times actual size. Then, the artwork was reduced photographically to actual

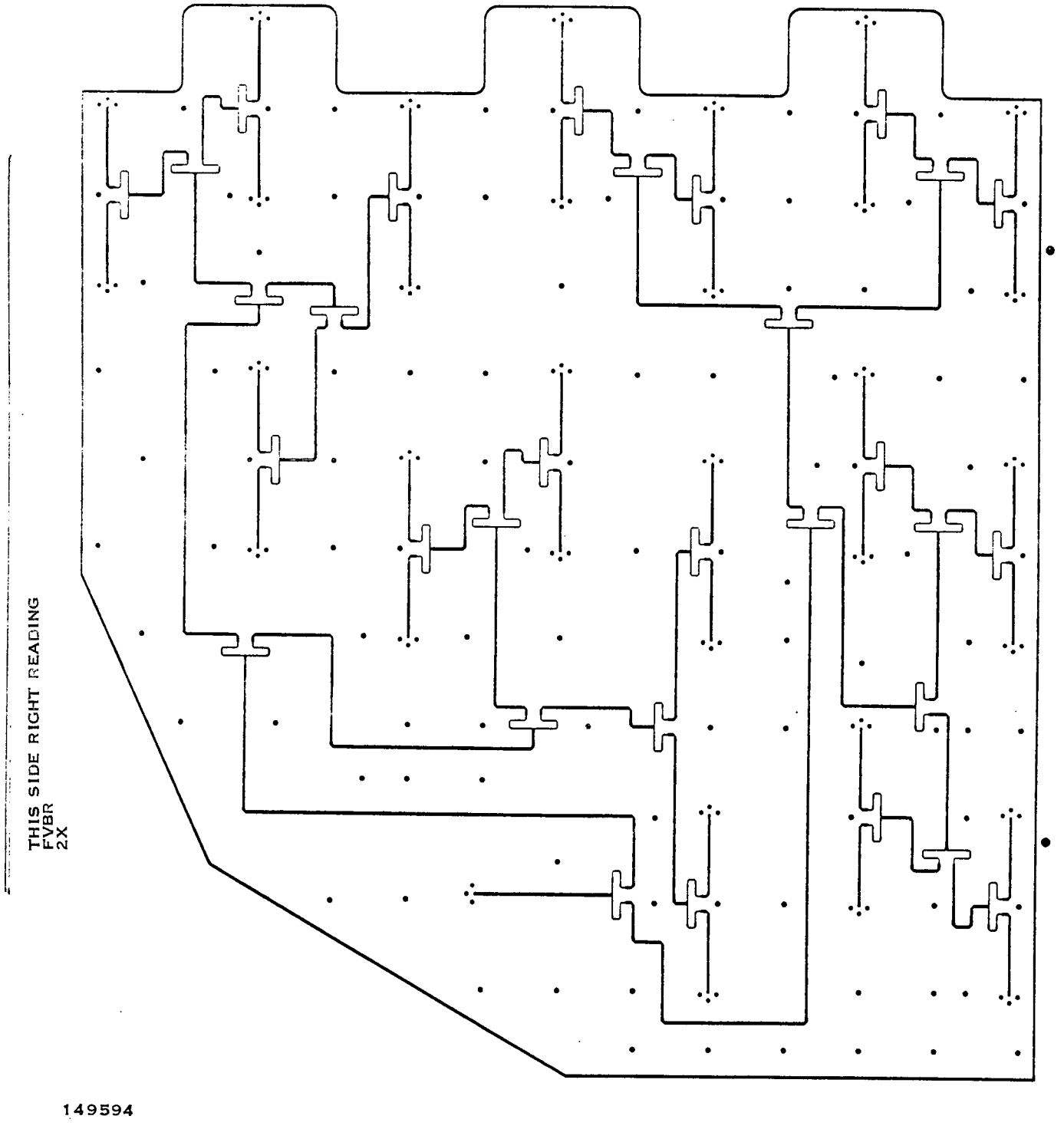


Figure 3-21. Photomask Used for Etching Transmit Manifold Quarter-Section

size to produce a negative which was used in the photoetching process. The artwork for one of the manifold quarter-sections is shown in Figure 3-21.

3. Fabrication Processes

The AESPA manifold was constructed using state-of-the-art stripline fabrication techniques. The most critical processes are the chemical bonding process and the plated-through hole process. These processes have been used for several years in the production of multilayer printed-circuit boards which are utilized in the packaging of high-density logic circuitry. Adaptation of these processes to the fabrication of microwave stripline circuitry has greatly reduced the weight of the stripline package and has improved the reliability of the finished unit.

There are seven basic steps in the overall fabrication process used in manufacturing the AESPA manifold. The first step is to etch the stripline circuit on the PPO dielectric. Special etching solutions are required for etching PPO because of its susceptibility to some chemicals. The weight savings obtained with this material were deemed sufficient to justify the added complexities and care required.

The second step involves the installation of connector pins and 100 Ω resistors in the split-tee power dividers. The third step involves the actual bonding of the two stripline layers. This involves application of a suitable adhesive to the board surfaces and curing under pressure at an elevated temperature. The curing cycle may be varied in time, pressure, and temperature to obtain the desired results. In the case of the AESPA manifold, initial bonding procedures produced excessive shrinkage of the PPO material. This problem was eliminated by varying the bonding temperature and press cycle without altering the integrity of the bond until the shrinkage was negligible.

The fourth step is drilling the holes required for grounding the outer ground-plane surfaces of the stripline circuit. These holes are spaced approximately a quarter-wavelength apart over the entire manifold surface. RF grounding is required around each of the input/output connections. The basic hole pattern is shown on the artwork in Figure 3-21. A photograph of a portion of the drilled transmit manifold ready to plate is shown in Figure 3-22. After drilling, the fifth step is the submission of the bonded dielectric boards in a plating bath and the deposition of a thin layer of copper on the exposed dielectric surfaces. The plating adheres to the outer surfaces and to the sidewalls of the holes drilled in step four, forming a conductive ground between the two copper ground-plane surfaces.

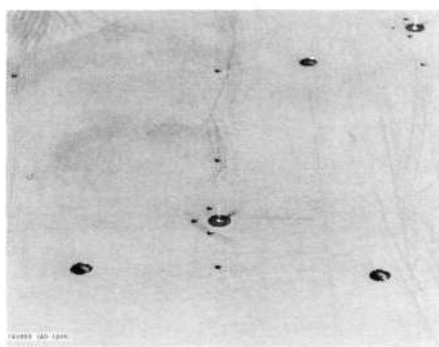


Figure 3-22. Bonded Manifold Section Before Plating

Step six is plating the copper with a thin layer of tin which has better corrosion resistance than copper. This added layer of tin facilitates step seven, soldering the press-on RF connectors, which completes the board.

Figure 3-23 is a simplified flow diagram of the steps required to process the AESPA manifold.

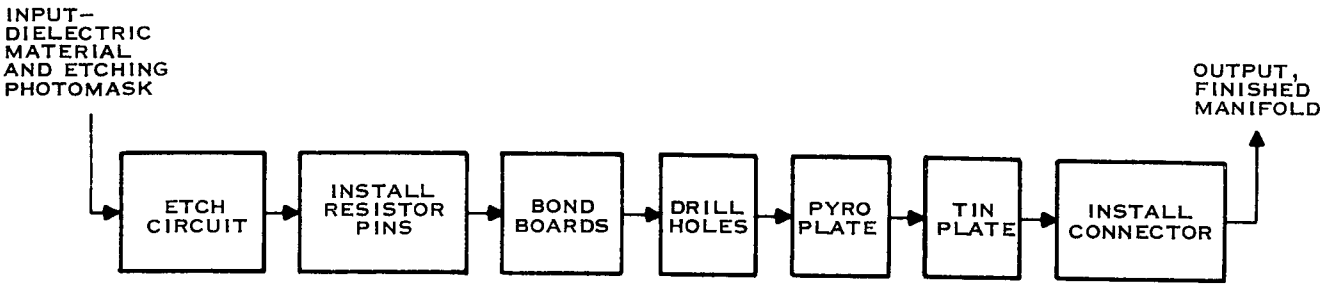


Figure 3-23. Simplified Flow Diagram of Steps Used in AESPA Manifold Processing

4. Manifold Performance

Electrical performance of the transmit manifold quarter-sections is evaluated through measurements of input and output VSWR, insertion loss, isolation between outputs, phase unbalance, and amplitude unbalance. The theoretical performance of a manifold consisting of cascaded split-tee power dividers is characterized by equal amplitude and equal phase signals at each of the 32 quarter-section outputs. All the transmitter input power will be transferred to the manifold outputs. In practice, losses due to impedance mismatch and energy dissipation in the dielectric substrate material are inevitable. Variations in the dielectric stripline material and bonding process, the RF connectors, and errors in development of the etching photomask result in phase and amplitude variations between the quarter-section outputs.

Figure 3-24 shows the measured VSWR of the four manifold sections over a 2.0- to 2.4-GHz frequency range. The VSWRs of the four manifold inputs vary from 1.40 to 1.75 at the AESPA transmit frequency of 2.282 GHz. The 128 output VSWRs vary between 1.15 and 1.55 at the AESPA transmit frequency. These values are well within the AESPA design goal of 2.0.

Fabrication tolerances can easily account for the minor variations in VSWR. The AESPA manifolds were fabricated in the Texas Instruments production fabrication shop and the variations shown in Figure 3-24 are typical of the expected performance of production units. These production processes are still being refined and improved units can be expected in the near future. The

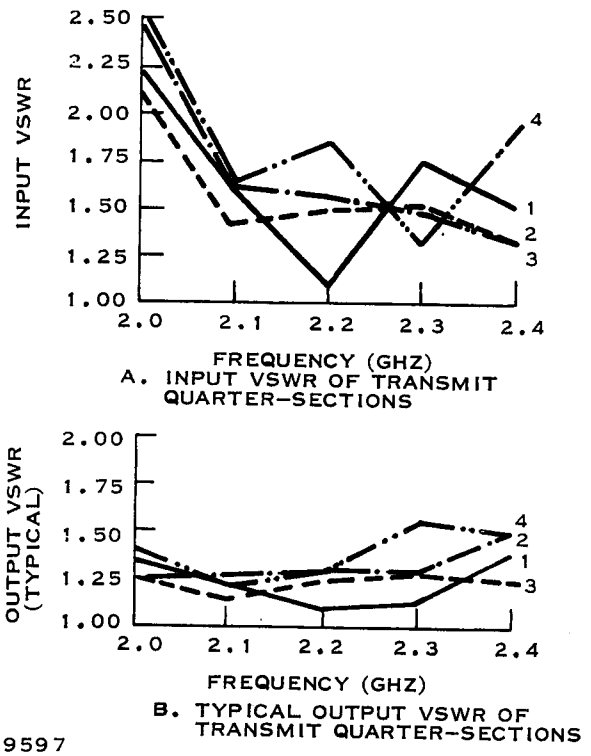


Figure 3-24. Measured Input and Output VSWRs of Transmit Manifold Quarter-Sections

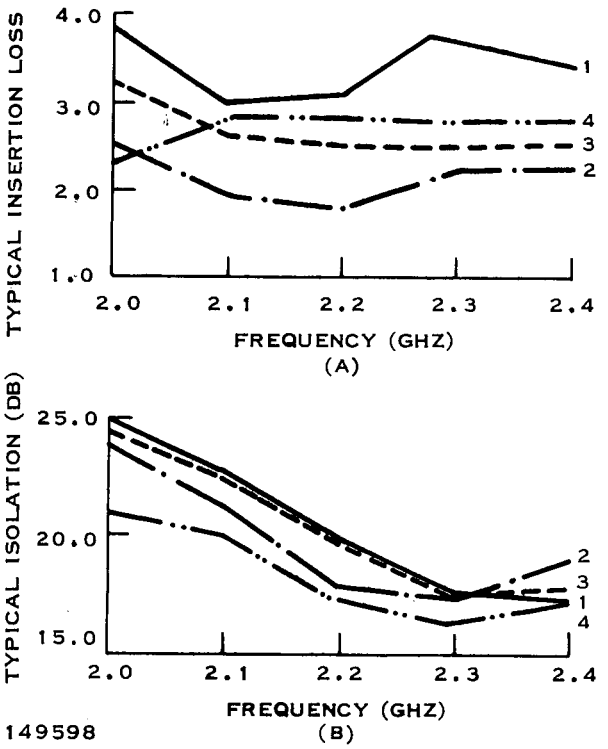


Figure 3-25. Measured Isolation and Insertion Loss of Transmit Manifold Quarter-Sections

insertion loss of the transmit manifold quarter-sections is shown in Figure 3-25A. Stripline insertion loss primarily depends on the electrical properties of the stripline dielectric substrate material and is proportional to the length of the transmission line paths. The path length in the AESPA transmit manifold is approximately 40 inches and the input signals travel through five levels of split-tee power dividers. The loss of 50 Ω stripline in PPO dielectric material at 2.282 GHz is approximately 0.5 dB per foot. The loss through each level of split-tee dividers is 0.2 dB. Using these values, the expected loss of the manifold quarter-sections is 2.6 dB. The median loss of the AESPA quarter-sections is 2.5 dB as shown in Figure 3-25A. This compares favorably with the expected losses. Quarter-section number one has approximately 1 dB more loss than the other three quarter-sections. X-rays of this quarter-section indicate that some contamination of the dielectric substrate occurred during the plating process. This quarter-section was the first fabricated and this problem was corrected in the remaining quarter-sections. The 1.0-dB loss difference has neglible effect on the overall array performance as evidenced in the sum and difference radiation patterns shown in Figure 3-14.

The isolation between adjacent manifold outputs is shown in Figure 3-25B. Isolation between outputs is of minor importance as long as the MIC transmit modules are impedance-matched. However, the effect of large impedance mismatches resulting from module failure or mutual coupling as the array is electronically steered off-boresight is greatly reduced by the isolation provided between manifold outputs. Reflected energy in the case of the isolated manifold is absorbed in the isolation resistors contained in the split-tee power dividers. Typical isolation of 17 dB is provided in the AESPA transmit manifold. This is more than sufficient to ensure the satisfactory performance of the AESPA array.

The remaining manifold performance parameters are the phase unbalance and the amplitude unbalance between outputs. These errors affect the symmetry and sidelobe level of the sum pattern and the symmetry and null depth of the difference radiation pattern. Measured data for the manifold quarter-sections are shown in Table 3-2. The worst case amplitude unbalance is 0.6 dB and the worst case phase error is 6.0 degrees. These errors are distributed randomly across the array surface and are not large enough to affect the overall array radiation patterns. The magnitude of the measured errors lies well within the expected results.

Three 180-degree hybrids interconnected with semiflexible cable were used to combine the outputs of the four manifold sections (Figure 3-26). Figure 3-27 shows the complete manifold antenna combined with the plywood antenna-range mounting structure.

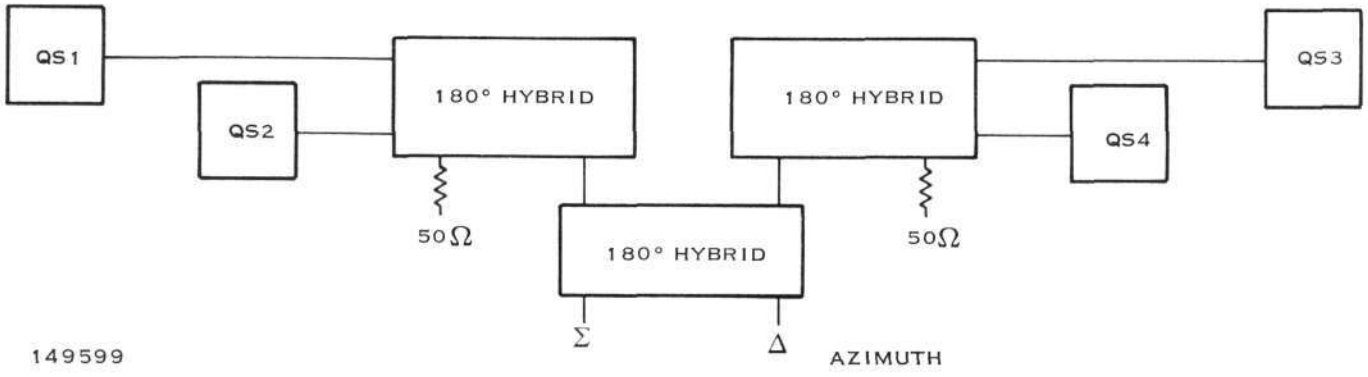


Figure 3-26. Interconnections of Transmit Manifold Quarter-Sections Diagram

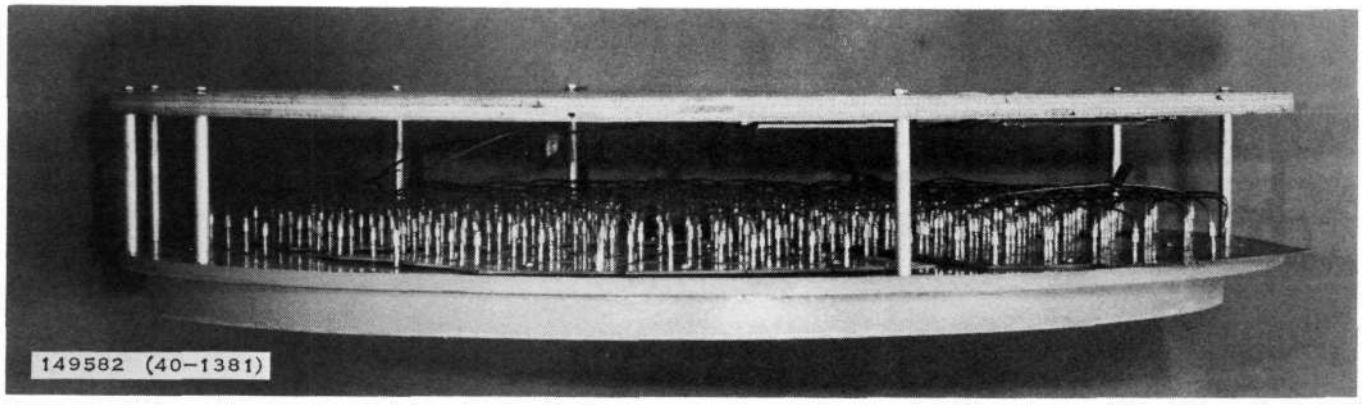


Figure 3-27. Transmit Manifold and Interconnecting Cables, Side View

TABLE 3-2. MEASURED TRANSMIT MANIFOLD QUARTER-SECTION PHASE AND AMPLITUDE UNBALANCE.

A. Maximum Amplitude Unbalance (±dB)

	Quarter Section			
Frequency	1	2	3	4
2.1	0.4	0.4	0.4	0.4
2.3	0.3	0.6	0.6	0.6

B. Maximum Phase Unbalance (± Degrees)

	Quarter Section			
Frequency	1	2	3	4
2.1	4.5	6.0	5.0	3.0
2.3	5.0	4.0	5.0	4.0

The overall performance of the transmit manifold is evaluated through gain, impedance, and radiation pattern evaluation of the complete 128-element spiral array and manifold combination.

C. Module Development

Figure 3-28 shows a simplified functional block diagram of the module which is capable of simultaneous transmission and reception. Separate phase shifters are required in the transmitter and receive channels. The module size, 6.35 by 7.36 cm, is dictated by the array grid. The layout is in two layers with the transmitter and receiver in separate sections. Module performance goals are listed in Table 3-3.

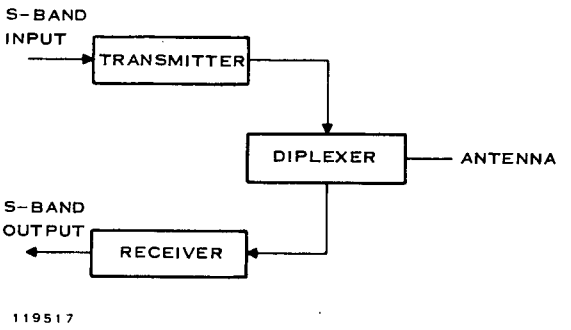


Figure 3-28. Simplified Module Block Diagram

TABLE 3-3. TRANSMITTER AND RECEIVER PERFORMANCE GOALS

Transmitter	
Frequency	2282 ±30 MHz
Output power	≥1.0-W CW
Gain	>22 dB
Input VSWR	<1.3:1
Efficiency of power chain	>25 percent
Phase errors	<10 degrees maximum
	<5 degrees rms
Phase linearity	±5 degrees (maximum)
Receiver	
Frequency	2101 ±30 MHz
Amplifier noise figure	<4.5 dB
Gain	>23 dB
Transmitter frequency rejection	>40 dB
Phase errors	<5 degrees rms
	<10 degrees maximum
Phase linearity	±5 degrees (maximum)

Figure 3-29 is a more detailed functional block diagram of the module. Nominal signal levels are given in dBm. The module is driven by a 15-mW S-band signal from the transmit manifold. The initial circuit in the transmitter is a 3-bit, diode-switched line phase shifter driven by TTL integrated circuits. The signal from the phase shifter is fed to a three-stage S-band power amplifier. The first two stages of the amplifier operate class-A and the last stage class-C. The amplifier has an output of approximately 1.3 W and a gain of 19 dB. The output of the power amplifier is coupled to the transmitter filter and is then routed to the circulator. This filter provides a minimum of 20-dB attenuation to noise in the receive band that is generated in the power amplifier. The output of the transmit filter is coupled to the antenna by way of the diplexer. A minimum of 1 watt is required at the antenna.

Receive signals enter the circulator and are routed to the receive filter. This filter provides 40-dB rejection to any signal in the transmit band. The output of the filter is fed to an S-band small signal amplifier. This amplifier provides 27 dB of gain with a noise figure of 4.5 dB. The

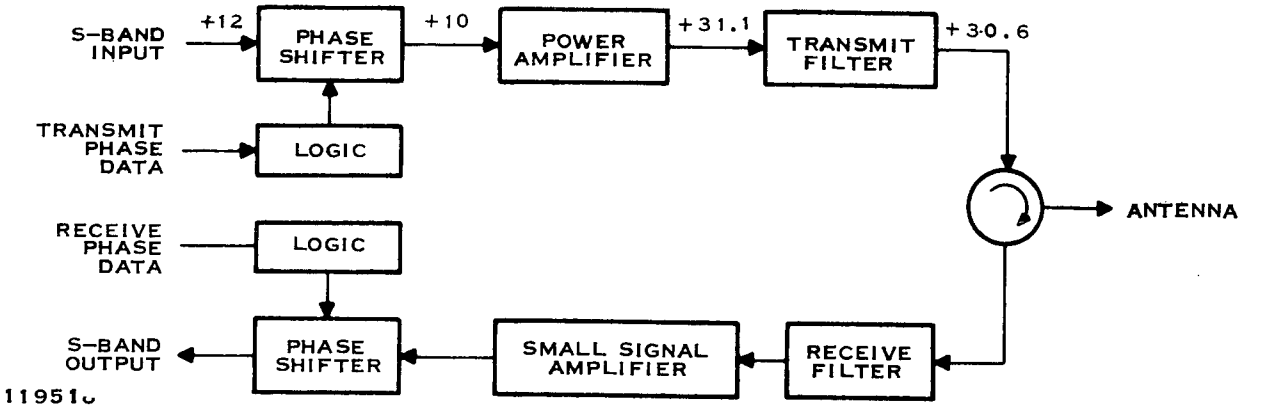


Figure 3-29. Module Block Diagram

signal from the amplifier is coupled to a 3-bit phase shifter similar to the transmit phasor. The design of each of the circuits is discussed and test results for the module and the circuits are presented in Subsection III.C.1.

1. Phase Shifter

A three-bit phase shifter is required in the transmitter and in the receiver. Both phase shifters are required to give a full 360-degree phase shift in 45-degree steps. The two center frequencies involved (2.101 GHz for the receiver and 2.282 GHz for the transmitter) are very close, but it was believed that separate phase shifters should be designed in an attempt to achieve optimum performance from both.

The original design goals set up for the two phase shifters were

A	Insertion loss	2.0 dB
b.	Input and output VSWR	1.5:1
c.	Phase accuracy	5.0 degrees rms

Several phase-shifter types are capable of meeting these goals; however, only two types, loaded line and switched line, are amenable to small size and low power consumption. Of these two, the switched-line type was selected because it is the most straightforward from the design and production viewpoints. A simplified switched line phase shifter is shown in Figure 3-30. The figure indicates that for a fixed length, ℓ', the phase shift is determined by $\ell - \ell'$. Table 3-4 gives line lengths (ℓ) for the 45-, 90- and 180-degree bits for the transmit and receive phase shifters. The length ℓ' is fixed at 1.8 mm for all three bits in both phase shifters. Also shown in the table is the length of the quarter-wavelength chokes used for bias lines. The schematic of the 3-bit, switched-line phase shifter is shown in Figure 3-31.

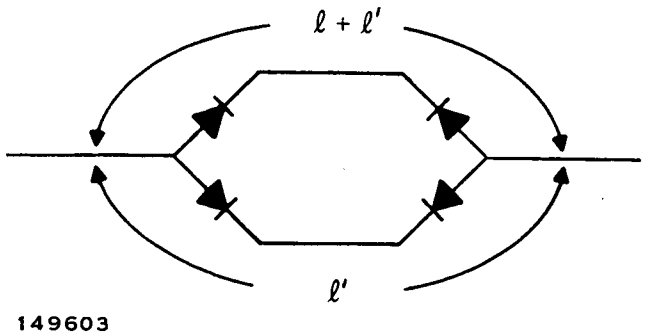


Figure 3-30. Simplified Switched-Line Phase Shifter

TABLE 3-4. LINE LENGTHS

	Transmitter	Receiver
45-degree bit	8.30 mm	8.86 mm
90-degree bit	14.80 mm	15.92 mm
180-degree bit	27.80 mm	30.04 mm
λ/4 lines	13.55 mm	14.72 mm

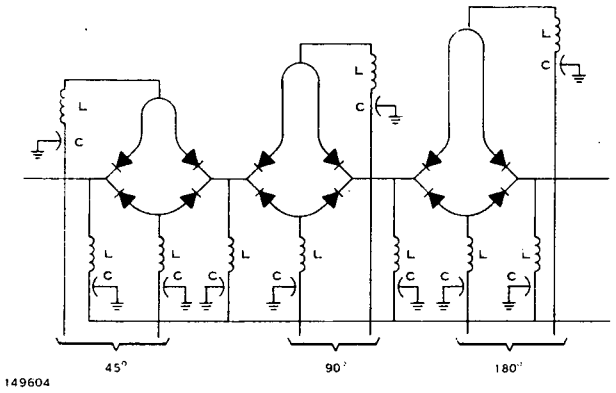


Figure 3-31. Three-Bit Switched-Line Phase Shifter Schematic

Assuming that the switching diodes do not affect the performance, the only other parameter that affects performance is the line lengths. The ideal diode for this type phase shifter has as low forward-bias resistance as possible, since for the most part this resistance determines the insertion loss of the phase shifter. The diode should have a low reverse-bias capacitance, since this capacitance determines the isolation between the ON and OFF lines. It becomes obvious that some tradeoff must be made between diode resistance and capacitance.

The MPN 3201 diode phase shifter was chosen because of its low forward-bias resistance, its low reverse-bias capacitance (providing adequate isolation), its availability in chip form, and its low cost. Figure 3-32 shows a resistance curve versus forward-bias current. The reverse-bias capacitance for this diode in chip form remains constant at 0.15 pF for all reverse-bias voltages at frequencies above 1 GHz. The diode chip measures approximately 0.51 mm^2 which permits the alloying of the device directly to the 50 Ω line on the substrate. This eliminates mounting problems connected with a packaged diode. Since the diode is a production item, it is available at low cost. This is of particular importance to array cost.

A phase shifter driver is required for diode switching. This circuit must be capable of accepting a serial input and of giving parallel outputs. The driver must also be capable of providing adequate forward-bias currents and reverse-bias voltages to the diodes. Each phase shifter bit requires complementary driving signals. All of this is accomplished by using standard Texas Instruments 5400-series integrated circuits and 2N2222 transistors. A schematic of this driver is shown in Figure 3-33. The SN5493 counter accepts the serial input and gives three parallel outputs; these three outputs drive the SN5475 holding register. The three holding-register outputs, plus their complements, drive the diodes in the phase shifter. Built on the same substrate is a 2-V voltage regulator. The 2 volts are applied to the anodes of all diodes in the phase shifter. This ensures that the diodes are either forward- or reverse-biased at all times. The voltage at the output of the holding register will be 0.2, or 4.0 volts, depending on whether the output is a logical zero or a

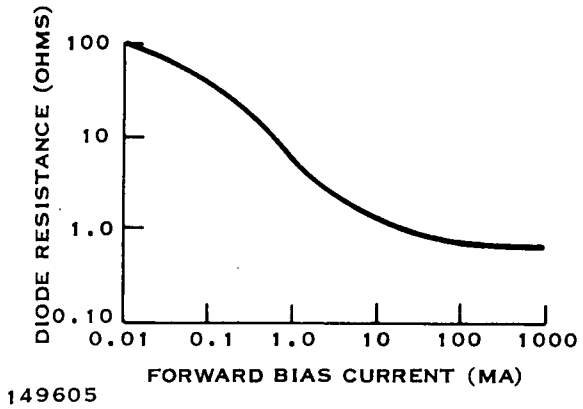


Figure 3-32. Diode Resistance Versus Forward Bias Current

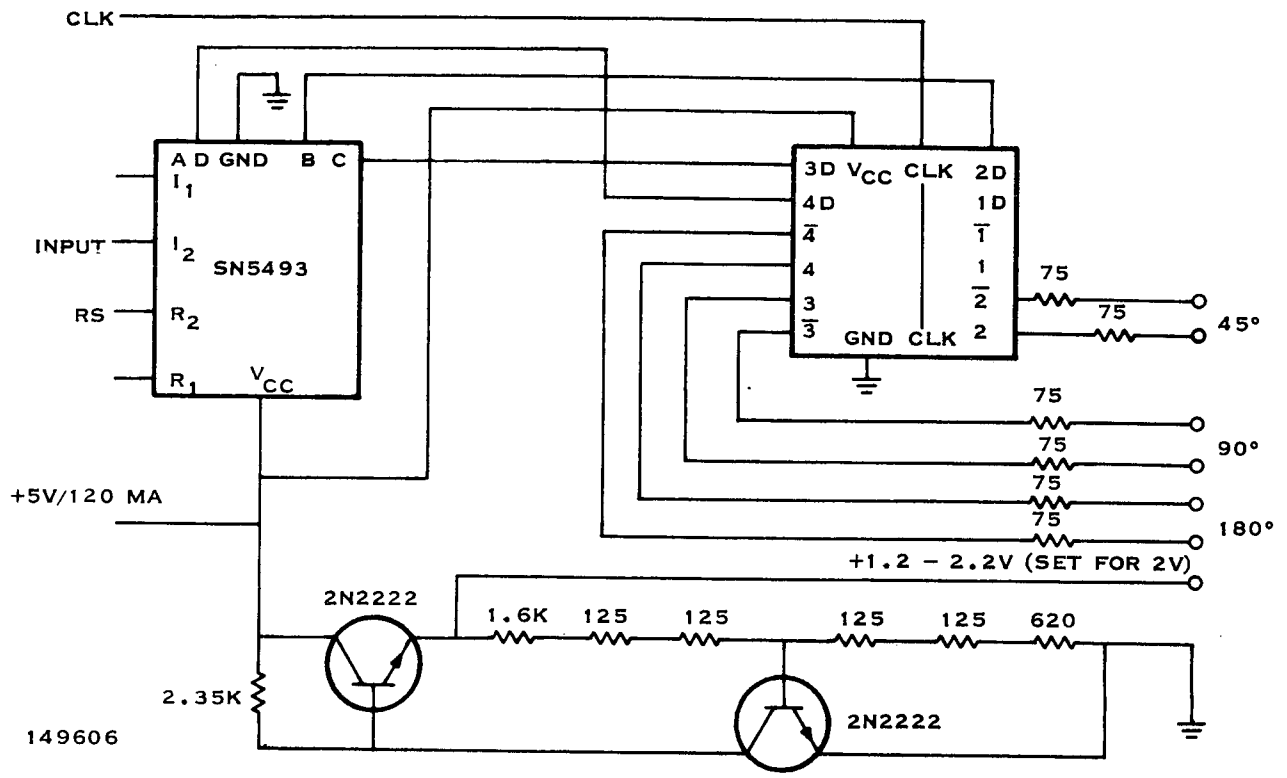


Figure 3-33. Phase Shifter Driver Schematic

logical one. With a logical zero at the output, the diodes in the respective phase shifter bits will be forward-biased. The forward-bias current is limited by the 75 Ω series resistors in the driver circuits. Using a diode voltage drop of around 0.7 V, the total current drawn by the two parallel diodes in the ON line will be approximately 15 mA, or 7.5 mA, per diode. The reverse-bias voltage on the diodes in the OFF line will be 2.0 volts which is sufficiently high to prevent clipping of the RF signal.

The phase shifter insertion loss is made up of diode losses, plus conductor and mismatch losses. The diode resistance can be found using the diode resistance versus current curve in Figure 3-32. A diode current of 7.5 mA will give a diode resistance of approximately 1.6 Ω which corresponds to an insertion loss of 0.28 dB per diode. Since there are six diodes in series with the transmission line at all times, the insertion loss caused by the diodes is approximately 1.7 dB. Allowing 0.3 dB for conductor and mismatch losses, the total phase shifter loss should be around 2.0 dB.

Photographs of the two phase shifters are shown in Figures 3-34 and 3-35. Figure 3-34 shows the transmitter phase shifter and its driver. Figure 3-35 shows the receiver phase shifter and its driver. Both phase shifters and both drivers are on 0.51 mm thick unglazed alumina substrates. The diodes in the phase shifters and the integrated circuits and transistors in drivers are alloyed to the substrate with gold-tin alloy. The 110-pF chip capacitors in the phase shifters are alloyed to the substrate with a gold-germanium alloy. The resistors in the driver circuit are deposited tantalum. The dimensions of each circuit are given in Table 3-5.

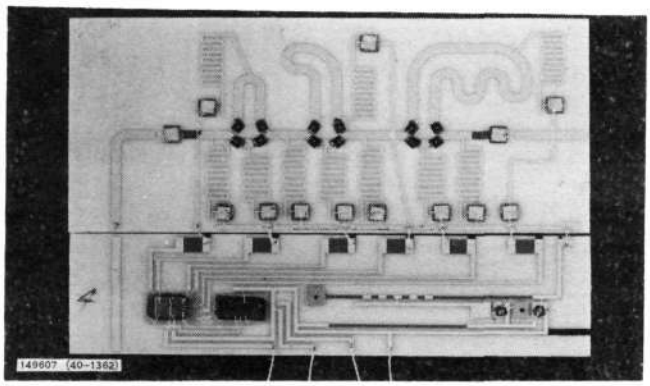


Figure 3-34. Transmitter Phase Shifter

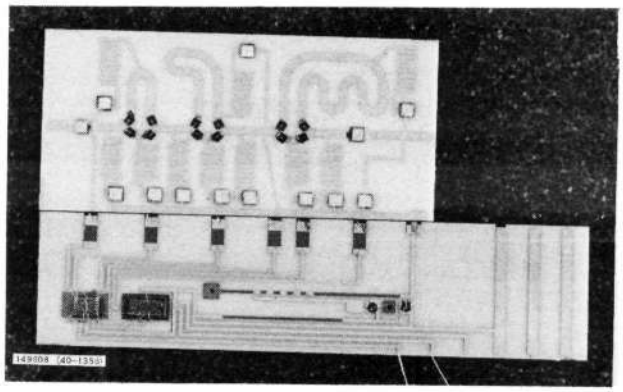


Figure 3-35. Receiver Phase Shifter

TABLE 3-5. SUBSTRATE DIMENSIONS

Substrate		Size in mm
Transmitter	Phase shifter	34.5 × 14.7
	Driver	34.5 × 8.5
Receiver	Phase shifter	30.0 × 14.2
	Driver	41.9 × 10.7

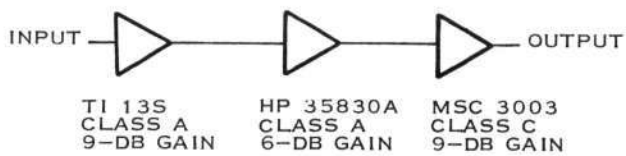


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Figure 3-36. Transmitter Block Diagram

2. Power Amplifier

A power amplifier (center frequency at 2.2825 GHz) in the transmit module amplifies the transmit signal between the manifold outputs and the antenna. The gain of this amplifier is subject to a tradeoff between the power required to drive the manifold and the module complexity. An original goal of 30 dB was set which would require four stages of amplification using available transistors. A three-stage amplifier provides adequate module gain and still keeps the required manifold drive signal at a reasonable level. Further, a three-stage amplifier as opposed to a four-stage amplifier would enhance module reliability, decrease power consumption, and decrease space requirements in the module.

The transmitter amplifier block diagram, along with device types, class of operation, and expected gains is shown in Figure 3-36. The TI13S transistor was chosen for the input stage because of its high gain characteristics at low power levels. The second stage utilizes an HP 35830A device which has very good medium-power characteristics. The TI13S and the HP 35830A devices are available in chip form, which is of particular importance in microwave integrated circuits (MIC). The Microwave Semiconductor Corporation MSC 3003 used in the output stage has excellent gain characteristics in the 1- to 3-watt region. This device has a very low thermal resistance which makes it particularly adaptable to high-temperature operation. The design goals for this amplifier are:

a. Gain, transmit band >24 dB

b. Gain, receive band <16 dB

c.	Power out	>1.3 watts
d.	Input VSWR	<1.4:1
e.	Efficiency	>30 percent
f.	Spurious outputs	<30 dB below transmit level, in receive band <50 dB below transmit signal
g.	Phase linearity	±5 degrees
h.	Amplitude linearity	±0.25 dB

The power amplifier was designed in two sections, a preamplifier and a postamplifier. The first two stages comprise the preamplifier and the last stage the postamplifier. The preamplifier has a 15-dB gain and the postamplifier, a 9-dB gain. Overall gain is 24 dB. The required drive level is 5.2 mW for 1.3 W output power.

a. Preamplifier

The preamplifier has 15-dB gain, or a 164-mW output for a 5.2 mW input. Because of the relatively low power levels involved, it was decided to operate both stages class-A.

To design the preamplifier, both transistors were characterized under the intended operating conditions, using the Hewlett Packard (HP) network analyzer. The S-parameters obtained from these measurements appear in Table 3-6.

TABLE 3-6. PREAMPLIFIER TRANSISTOR S-PARAMETERS

Frequency (GHz) TI13S	S_{11}		S_{12}		S_{21}		S_{22}	
2.0	0.55	164	0.0045	109	1.86	63	0.69	−9
2.1	0.56	162	0.0050	108	1.77	62	0.69	−10
2.2	0.58	160	0.0051	107	1.66	60	0.69	−11
2.3	0.59	158	0.0054	105	1.59	59	0.69	−12
2.4	0.60	157	0.0057	103	1.53	56	0.69	−13
2.5	0.62	157	0.0060	101	1.47	54	0.69	−14
HP35830A								
2.0	0.54	178	0.017	53	1.61	38	0.33	−63
2.1	0.54	175	0.018	51	1.52	36	0.33	−63
2.2	0.55	173	0.018	51	1.47	31	0.33	−63
2.3	0.54	172	0.019	50	1.42	29	0.34	−64
2.4	0.54	168	0.019	48	1.37	25	0.35	−65
2.5	0.55	167	0.020	46	1.34	24	0.35	−65

The S-parameters were then used in conjunction with the design and optimization computer program (CAIN) to obtain a circuit design. The finalized circuit obtained from the computer is shown in Figure 3-37. The matching elements are MIC transmission lines. The

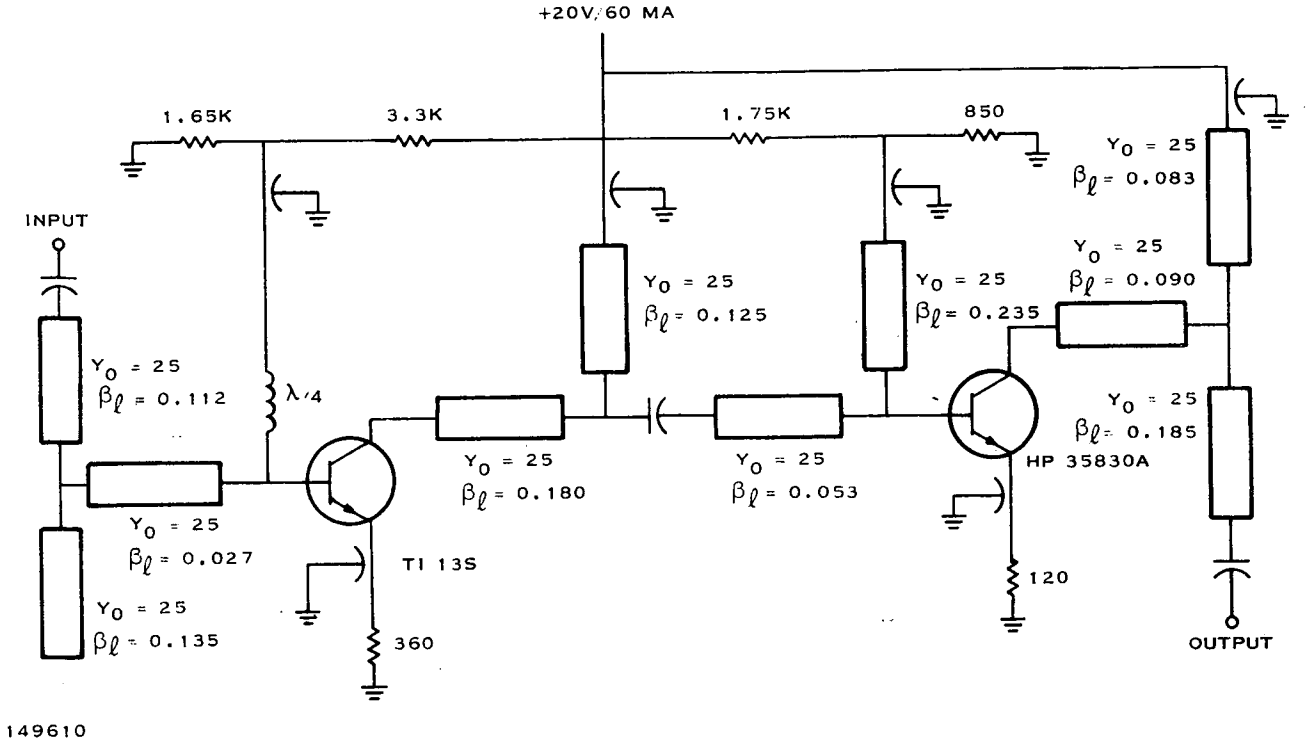


Figure 3-37. Transmitter Preamplifier

TABLE 3-7. PREAMPLIFIER ELEMENT DIMENSIONS

Element No.	Dimensions in mm
1	0.76 X 5.66
2	0.76 X 6.80
3	0.76 X 1.37
4	0.76 X 9.10
5	0.76 X 6.40
6	0.76 X 2.66
7	0.76 X 11.85
8	0.76 X 4.55
9	0.76 X 4.16
10	0.76 X 9.35

characteristic admittances and electrical lengths are shown next to each element. The line lengths and widths for 0.51 mm thick alumina substrate ($\epsilon_r = 9.6$) are shown in Table 3-7. The bypass and coupling capacitors are thin-film lumped elements. The resistors are thin-film tantalum which were deposited during substrate processing.

The theoretical performance of the preamplifier is given in Table 3-8. Gain, input VSWR and output VSWR are listed for frequencies ranging from 2.0 GHz to 2.5 GHz. The complete preamplifier is shown in Figure 3-38. The amplifier substrate is in two sections with the second-stage transistor (HP 35830A) mounted between the two sections. This transistor is on a beryllium oxide substrate for improved heat dissipation. A photograph of the substrate is shown in Figure 3-39. The emitter bypass capacitors are mounted on the same substrate and have gold ribbons bonded around the edges for ground connection. The overall amplifier measures 34.3 by 27.3 mm and the transistor carrier substrate measures 1.91 by 4.32 mm.

TABLE 3-8. THEORETICAL PREAMPLIFIER PERFORMANCE

Frequency (GHz)	Gain (dB)	Input VSWR	Output VSWR
2.000	12.65	1.835	3.137
2.020	12.81	1.803	3.025
2.040	12.97	1.772	2.925
2.060	13.16	1.742	2.780
2.080	13.35	1.711	2.653
2.100	13.55	1.681	2.521
2.120	13.75	1.650	2.375
2.140	13.95	1.620	2.232
2.160	14.14	1.589	2.090
2.180	14.33	1.557	1.948
2.200	14.49	1.525	1.800
2.220	14.63	1.493	1.664
2.240	14.74	1.460	1.530
2.260	14.82	1.427	1.405
2.280	14.85	1.393	1.289
2.300	14.85	1.360	1.187
2.320	14.81	1.328	1.097
2.340	14.71	1.297	1.046
2.360	14.57	1.268	1.103
2.380	14.40	1.242	1.185
2.400	14.18	1.220	1.271
2.420	13.94	1.203	1.356
2.440	13.65	1.190	1.442
2.460	13.33	1.183	1.525
2.480	12.99	1.183	1.603
2.500	12.62	1.188	1.678

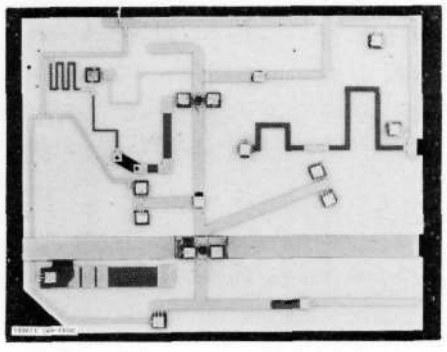


Figure 3-38. Assembled Preamplifier

b. Postamplifier

The postamplifier is a single-stage amplifier which uses the MSC 3003 transistor. This amplifier is required to give 1.3-watt output for 164-mW input, or a 9-dB gain. It was elected to operate this stage class-C to achieve maximum efficiency and stability. According to MSC published data, this device is capable of efficiencies of up to 40 percent so that for 1.3-w output, the transistor dissipates approximately 2.1 watts. The thermal resistance for this

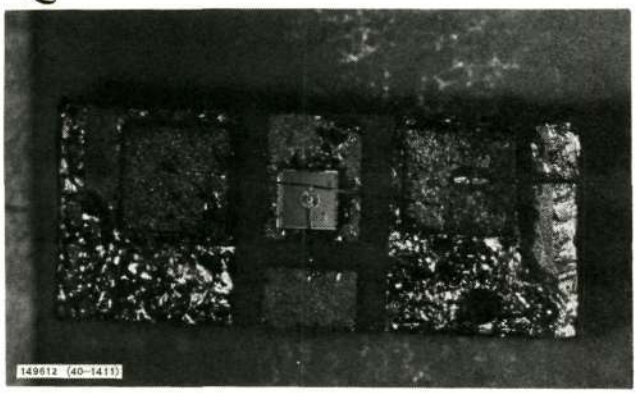


Figure 3-39. Transistor Carrier Substrate

TABLE 3-9. MSC 3003 IMPEDANCES

Frequency (GHz)	Input Impedance	Collector Load Impedance
2.2	5.5 + j13.0	5.5 + J0.0
2.3	5.5 + j13.5	5.0 – j1.5
2.4	5.5 + j14.0	4.5 – j2.8

transistor is 17°C/W which gives a junction temperature of 121°C for a case temperature of 85°C. This is well within the safe limits of the device.

To design the amplifier, the impedance parameters published by MSC and a Smith chart were used. The input and output impedances for 2.2, 2.3 and 2.4 GHz are given in Table 3-9. The input Smith chart plot is shown in Figure 3-40 and the output plot in Figure 3-41. During the initial design and evaluation phases of this amplifier, it was necessary to reduce the collector voltage from 28 to 20 volts. This was done to improve the low-power operation of the transistor. The impedance data published by MSC was for a collector voltage of 28 volts. The reduction in collector voltage changed the input and output impedances which required a corresponding change in the input and output matching networks. The circuit which

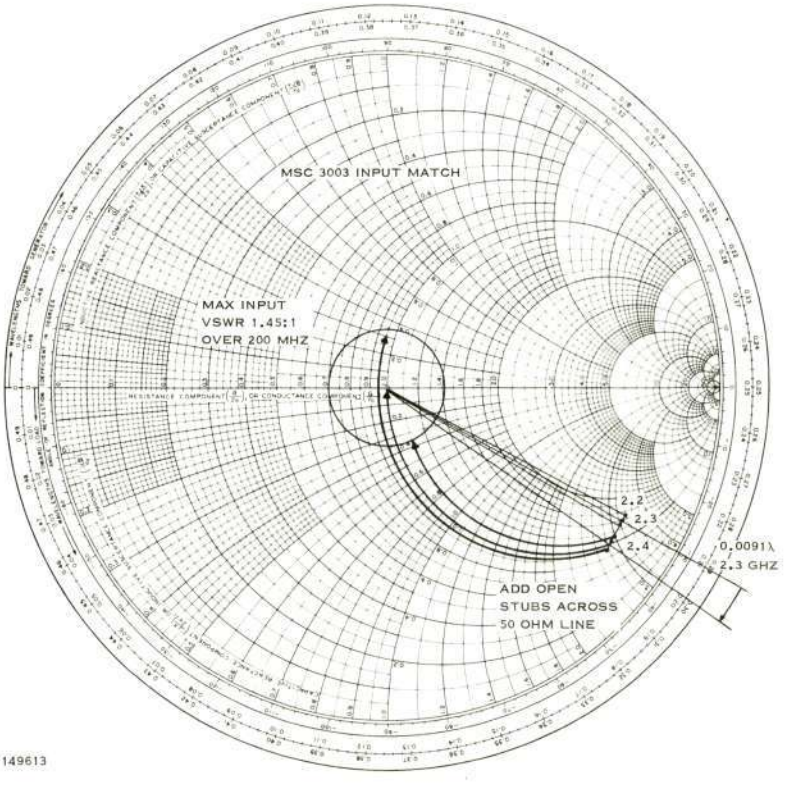


Figure 3-40. Smith Chart Input Plot

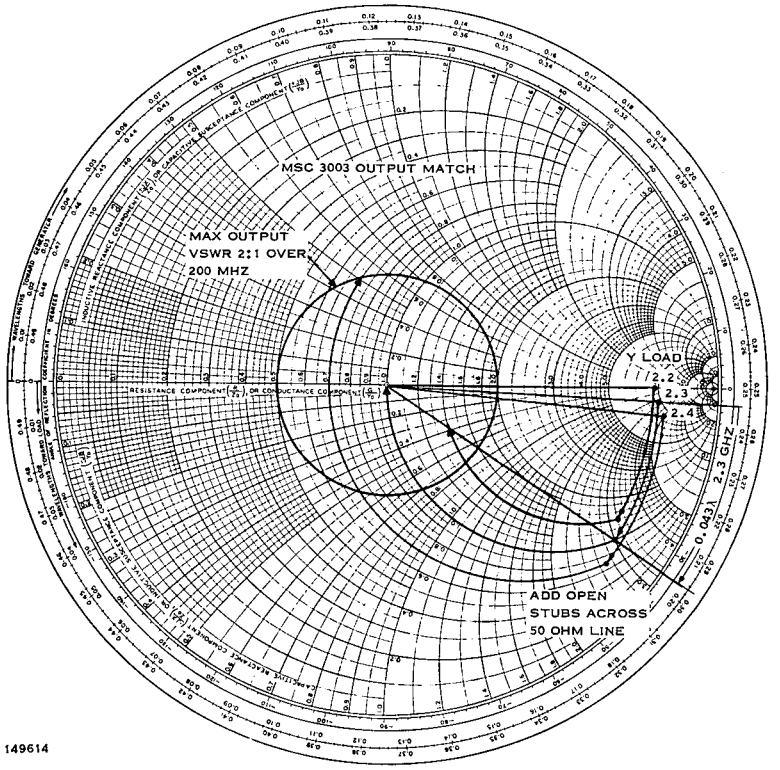


Figure 3-41. Smith Chart Output Plot

resulted is shown in Figure 3-42. The characteristic admittances and electrical lengths for 0.51 mm thick alumina substrate are shown adjacent to the elements. The dimensions of the elements are given in Table 3-10. The lengths of the open stubs were made adjustable to compensate for impedance differences which might exist from transistor to transistor. A photograph of the amplifier is shown in Figure 3-43.

The amplifier was built on two separate substrates, since the transistor must be alloyed directly to the module case. This minimizes module case-to-transistor case thermal

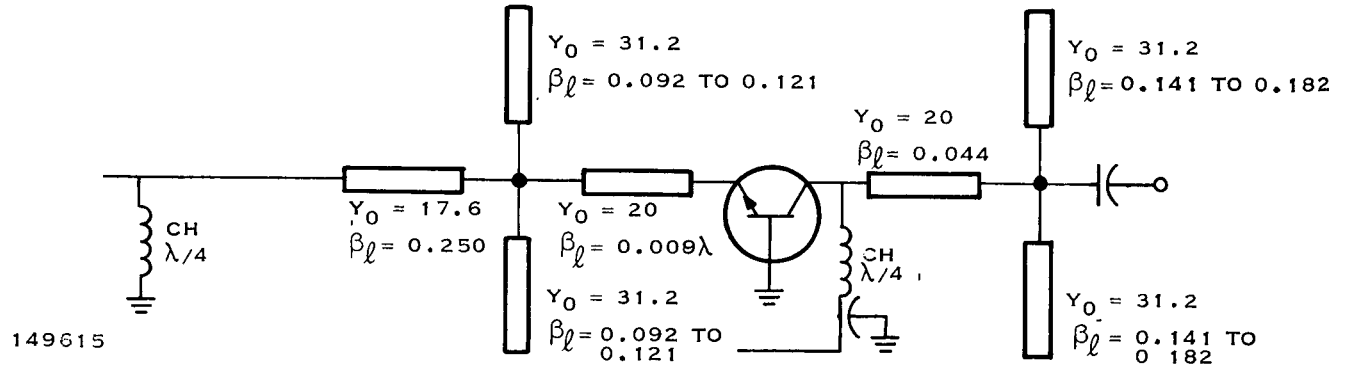


Figure 3-42. Postamplifier Schematic

TABLE 3-10. POSTAMPLIFIER ELEMENT DIMENSIONS

Element Number	Width (mm)	Length (mm)
1	0.38	12.7
2	0.79	4.8 to 6.3
3	0.79	4.8 to 6.3
4	0.51	0.50
5	0.51	2.4
6	0.79	7.4 to 9.5
7	0.79	7.4 to 9.5

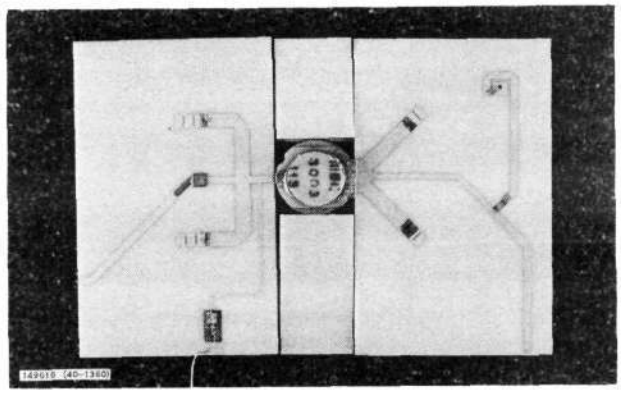


Figure 3-43. Postamplifier Photograph

resistance. The input matching network is on one substrate and the output network is on the other. Both substrates measure 15.0 by 24.5 mm.

c. Low-Noise Amplifier

The array noise figure is set by the module receiver noise figure and gain, plus the antenna loss. The three noise-figure determining circuits in the module receiver are the diplexer, receiver filter and the low-noise amplifier. The low-noise amplifier has sufficient gain to render following-circuit noise figures insignificant. The two most important design criteria for this amplifier are noise figure and gain. Amplifier gain can be controlled by the number of stages, while noise figure is limited by the noise figures of the transistors.

The transistor selected for use in the first and second stages is the Hewlett Packard 35820A. This device is available with a guaranteed noise figure (NF) of less than 4 dB at 2 GHz. When impedance matched and biased for minimum NF, this device has a gain of approximately 7 dB at 2.1 GHz. When matched and biased for maximum gain, the device is capable of approximately 10-dB gain. It was decided to limit the number of stages in the amplifier to three. The TI13S transistor was selected for the third stage. This device has a gain of approximately 10.5 dB at 2.1 GHz. The three-stage amplifier has gain of approximately 27 dB which should be sufficient to buffer the noise figure of following circuitry.

The Hewlett Packard published S-parameters for the HP 35820A are given in Table 3-11. The S-parameters for the TI 13S transistor are shown in Table 3-6. Since both transistors are available in chip form, they can be alloyed directly to the substrate. This allows minimum amplifier size and reduces the possibility of parasitics sometimes associated with packaged devices.

The theoretical noise figure of the three-stage amplifier can be computed using the general equation for the noise figure of networks in cascade. The expected gain and noise figure of each stage is as follows.

	Gain (dB)	Noise Figure (dB)
First stage	7	4.0
Second stage	9.5	4.3
Third stage	10.5	6.0

TABLE 3-11. S-PARAMETERS FOR THE HP 35820A TRANSISTOR

Frequency (GHz)	S_{11}		S_{12}		S_{21}		S_{22}	
1.0	0.67	−159	0.04	40	5.1	91	0.44	−32
2.0	0.67	−164	0.065	52	2.8	78	0.45	−37
3.0	0.67	−168	0.085	52	2.0	61	0.47	−46
4.0	0.68	−173	0.125	45	1.5	50	0.51	−55

Using the general noise-figure equation, the overall noise figure was calculated to be approximately 4.6 dB.

The design of this amplifier was started by using an existing two-stage amplifier which had been designed to operate at 2.2 GHz. This amplifier utilized TI 13S transistors which have very close to the same S-parameters as the HP 35820A. The TI13S devices were replaced by the HP 35820A devices with no noticeable change in gain or frequency response. The amplifier was then tuned to 2.101 ±30 GHz. This was done by placing open stubs at various positions along the series matching lines. Lengths and widths of existing matching elements were varied. The end result was the addition of a single open stub along one of the series elements in the interstage matching network. The two-stage amplifier at this point displayed a gain of approximately 19 dB over the receive band. Next, the noise figure of the two-stage amplifier was optimized by varying the emitter currents and the input match while monitoring noise figure. The resulting amplifier had a 4.4-dB noise figure and an approximate 17-dB gain. A three-stage amplifier was then built, using the same matching networks utilized in the two-stage amplifier.

The complete three-stage amplifier is shown in Figure 3-44. The electrical lengths and characteristic admittances are shown adjacent to each element. The element dimensions for 0.51 mm thick alumina substrate ($\epsilon_r = 9.6$) are given in Table 3-12. All capacitors in the amplifier are 110-pf, thin-film lumped elements. The resistors are thin-film tantalum deposited on the substrate. A photograph of the amplifier appears in Figure 3-45. The finished amplifier measures 24.2 by 25.2 mm.

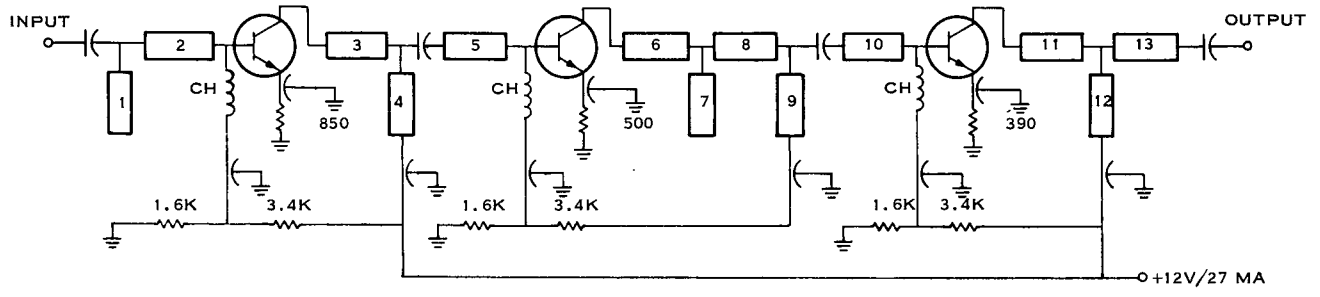


Figure 3-44. Low-Noise Amplifier Schematic

TABLE 3-12. LOW-NOISE AMPLIFIER ELEMENT DIMENSIONS

Element	Width (mm)	Length (mm)
1	7.6	76.0
2	6.1	30.0
3	7.6	75.5
4	7.6	73.0
5	7.6	67.4
6	7.6	57.0
7	7.6	22.8
8	7.6	21.6
9	7.6	73.0
10	7.6	67.4
11	7.6	101.0
12	7.6	23.1
13	8.4	123.0

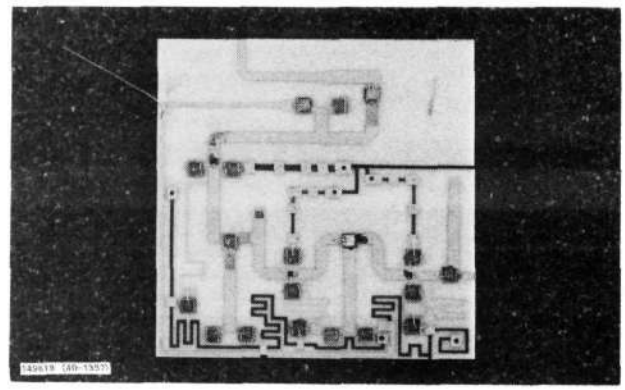


Figure 3-45. Low-Noise Amplifier Schematic

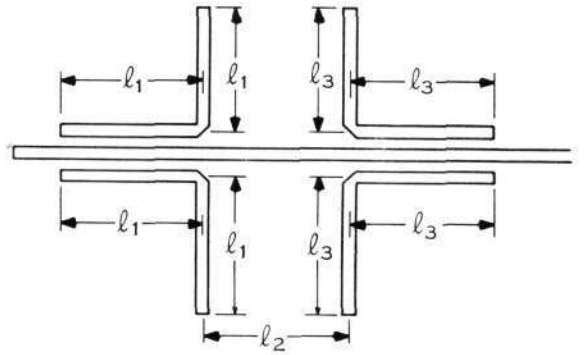
d. Filters

Two filters are used in the module design. One is located in the transmitter section after the power amplifier. This filter provides attenuation to any noise generated in the amplifier in the receive band. The other is located in the receiver section before the receiver amplifier. This filter provides attenuation to the transmit signal. This signal must be reduced to a level sufficiently low that no blocking takes place in the receiver amplifier and that no generated spurious signals fall in the receive band.

(1) Transmitter Filter

The basic requirement of the transmit filter is to attenuate noise output from the transmit amplifier and which falls in the receive band. This filter should present as little attenuation to the transmit signal as possible. Attenuation from this filter to the transmit frequency requires the transmit amplifier output to be correspondingly higher for a given power at the diplexer. The amount of attenuation required in the receive band is based on the transmitter amplifier noise figure and gain at the receive frequency and the VSWR of the antenna at the receive frequency. For a 5-dB noise figure, a 23-dB gain, and an antenna VSWR of 1.5:1, the transmitter filter is required to present at least 19-dB attenuation in the receive band.

Several filter types were considered for use in the transmitter. Of these, the band reject offered the best compromise between rejection in the receive band and insertion loss in the transmit band. The band reject filter (Figure 3-46) utilizes four spurline filters. Since a single spurline filter is capable of a limited amount of rejection over a very limited band, two sets of these filters were used. The two spurline filters in each set achieve the rejection and two sets achieve the bandwidth. One filter set, tuned to 30 MHz above and the other to 30 MHz below the receive center frequency. The two filter sets were spaced a quarter-wavelength apart at the receive center frequency. The spacing between the coupled sections and the through-line was determined experimentally. This spacing determines the slope of the reject skirts and, to a somewhat lesser extent, the amount of rejection in the reject band. This spacing was adjusted to



$\ell_1 = \lambda/4$ AT F_R +30 MHZ
$\ell_2 = \lambda/4$ AT F_R
$\ell_3 = \lambda/4$ AT F_R −30 MHZ
F_R = 2.101 GHZ

149619

Figure 3-46. Notch Filter

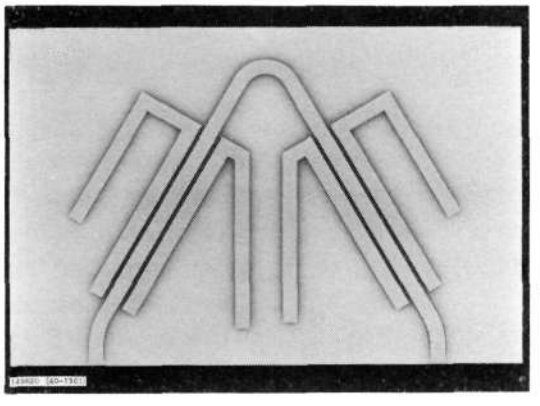


Figure 3-47. Transmitter Filter

give the best compromise between rejection in the receive band and insertion loss in the transmit band.

The filter was fabricated on a 1.02 mm thick alumina substrate to further minimize losses. The lengths of the filter element l_1, l_2 and l_3, shown in Figure 3-46, are 14.0, 14.2, 14.4 mm. The line widths are all 1.02 mm. This corre sponds to a characteristic impedance of 50 Ω for 1.02 mm thick alumina ($\epsilon_r = 9.6$). Figure 3-47 is a photograph of the filter. The filter measures 38.1 by 25.4 mm.

(2) Receiver Filter

The purpose of the receiver filter is to reduce the transmit signal to such a level that no blocking occurs in the receiver amplifier and no cross modulation or intermodulation products are generated which fall in the receive band. It was first thought that this filter must present at least 50-dB rejection to the transmit signal. However, after cross-modulation and intermodulation tests were performed on the receiver amplifier it was found that this rejection could be reduced to 40 dB. This is assuming a VSWR of 2:1 at the antenna which results in a 10-dB effective isolation in the diplexer.

Waveguide, coaxial, stripline, lumped elements and microstrip filter types were considered for this application. Of these, waveguide and coaxial types are too large to fit the module size limitation. The performance of lumped-element filters is limited by the Qs of the components used in the filter. Components suitable for application at this frequency and size limitation have been found to be very low Q, so this filter type could not provide the desired performance. Microstrip and stripline filters were fabricated and tested. These filters were interdigital bandpass types.

The stripline filter displayed excellent rejection characteristics but the in-band loss was considered too high for this module. Rejections of 50 dB were obtained with this type filter with in-band losses ranging from 2.5 to 3 dB. Since this filter was to be placed in front of the receiver amplifier, it was not used because such a loss would seriously degrade the

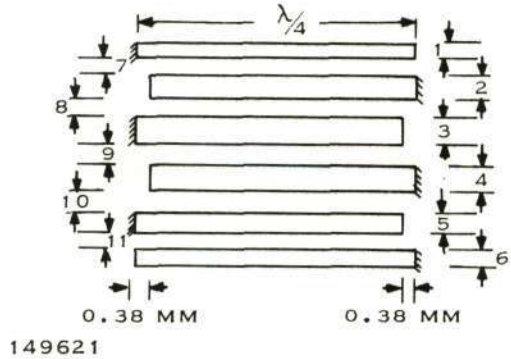


Figure 3-48. Six-Element Interdigital Filter

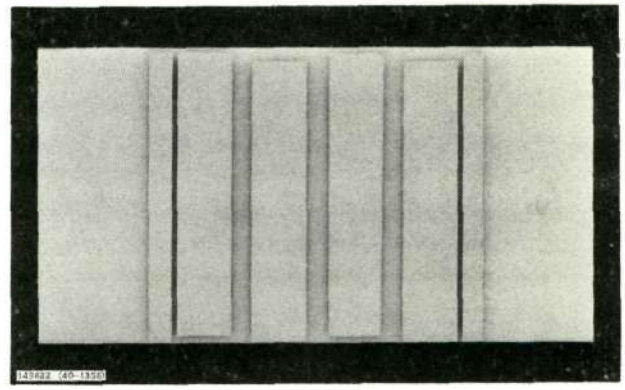


Figure 3-49. Receiver Filter

TABLE 3-13. RECEIVER FILTER ELEMENT AND GAP WIDTHS

Element Number	Element Width (mm)
1	0.89
2	2.14
3	2.14
4	2.14
5	2.14
6	0.89

Gap Number	Gap Width (mm)
7	0.25
8	0.89
9	1.02
10	0.89
11	0.25

module noise figure. The microstrip filter offers the best compromise between rejection and in-band loss; it can be made quite small and it is the most reproducible of the types considered.

The filter selected for use in this module is a six-element interdigital microstrip filter (Figure 3-48). The design of this type filter in this case was essentially experimental. The number of elements used determines the maximum rejection obtainable; the higher the number of elements, the higher the maximum rejection. As the number of elements increases, the in-band insertion loss increases. Six elements were used for this filter. This gives the required 40-dB rejection and minimizes in-band insertion loss. The element widths were arrived at from an identical filter design in stripline. The characteristic impedance of the elements were made to be identical with those in the stripline filter. The gap widths were determined experimentally. Several filters were fabricated and tested, using various gap widths. approximately the same relationship of stripline gap widths were maintained in the microstrip. Table 3-13 gives final gap and element widths for this filter. The open ends of the elements were cut back approximately 0.38 mm to compensate for the capacitive characteristic of open-ended transmission lines. The length of the filter is a quarter-wavelength at the middle of its bandpass. The filter was designed for a 160-MHz passband or a 2.05-GHz center frequency. The nominal length at this frequency is 13.7 mm. The completed filter shown in Figure 3-49 measures 13.7 by 25.4 mm.

e. Diplexer

The diplexer consists of a single three-port circulator. The requirements placed on this circulator are 20-dB minimum isolation and 0.4-dB maximum insertion loss over the receive and transmit bands.

Figure 3-50. Diplexer

The circulator used for this module was purchased from Trak Microwave Corporation. It is a lumped-element type which is the smallest type available at this time (Figure 3-50). The unit measures 19 by 19 by 12.7 mm, excluding connectors and the mounting bracket. This circulator is equivalent to the Trak Model 1420-1310 isolator, except all three ports are brought out to connectors and to connector locations which are altered to fit the module layout.

3. Design Evaluation

The design evaluation includes a summary of test results and a description of the tests. Areas where additional work would result in improved module performance are discussed in Section IV.

The module assembly sequence is shown in the photographs of Figure 3-51. The photographs show the transmitter, receiver, separation plate, diplexer and dc connector. The transmitter and receiver sides of the module are assembled with the separation plate between them. The last assembly step is the installation of the dc connector and the diplexer. This module design permits the independent building and testing of the transmitter and the receiver. Since the diplexer is mounted outside the module, it can be installed or removed at any time.

a. Summary of Test Results

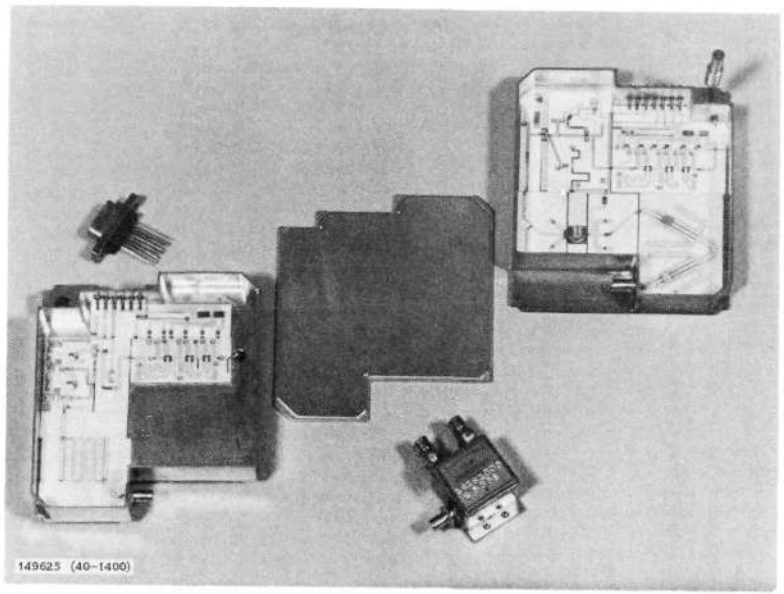
Test results for individual circuits and the completed module are presented in this subsection. Recommendations are made in Subsection III.C.5. These are based primarily on test results.

(1) Circuits

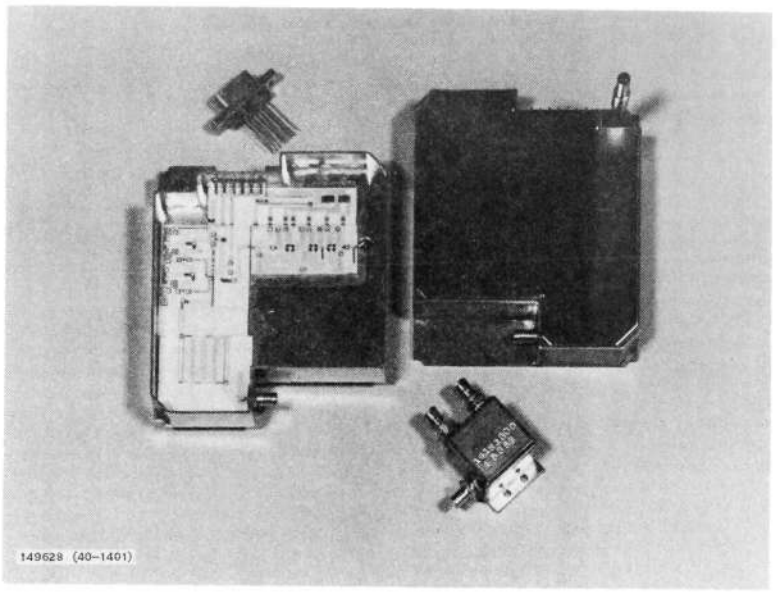
Pertinent test results for the phase shifters, power amplifier, low-noise amplifier, transmitter filter and receiver filter follow.

(a) Phase Shifters

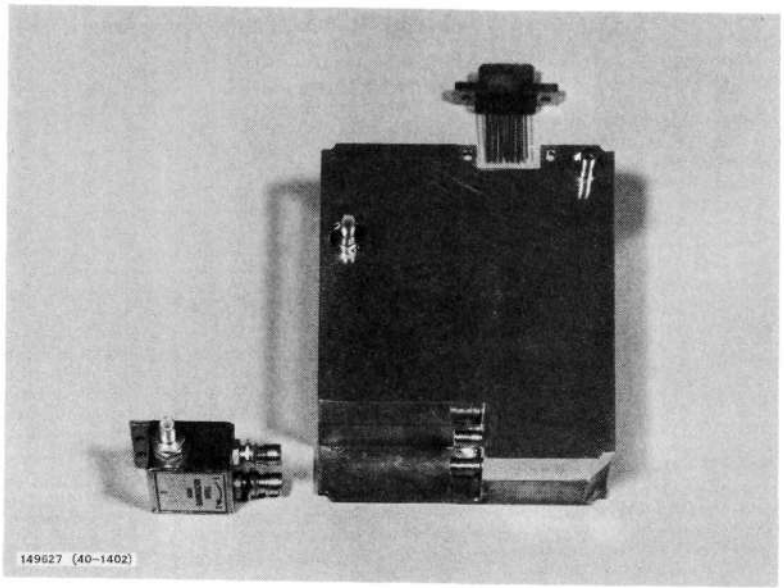
The phase-shift errors and insertion losses versus the desired phase shift for the transmitter phase shifter are shown in Figure 3-52. These data are plotted for 2.25, 2.28 and 2.31 GHz. The same receiver phase shifter characteristics are shown in Figure 3-53. The three plots are for 2.07, 2.10 and 2.13 GHz. Figure 3-54 gives the input VSWR versus the desired shift for transmitter and receiver phase shifters.



STEP 1



STEP 2



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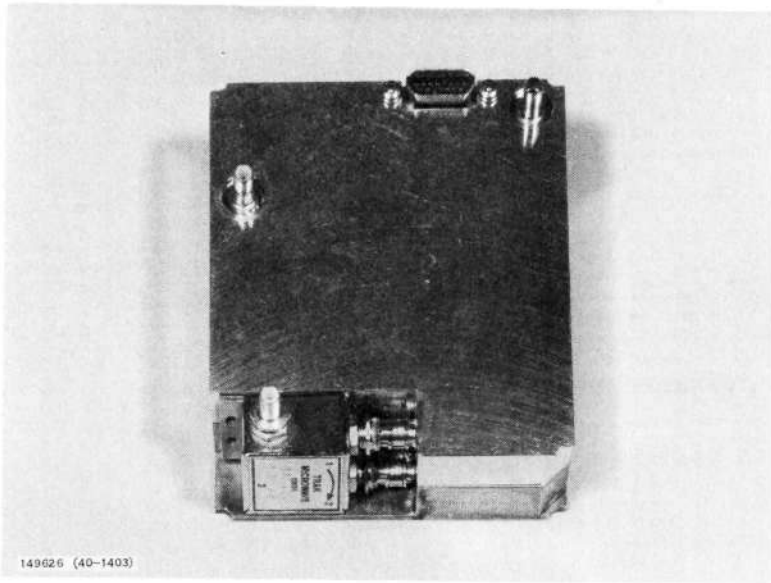
STEP 3



STEP 4

Figure 3-51. Module Assembly Sequence

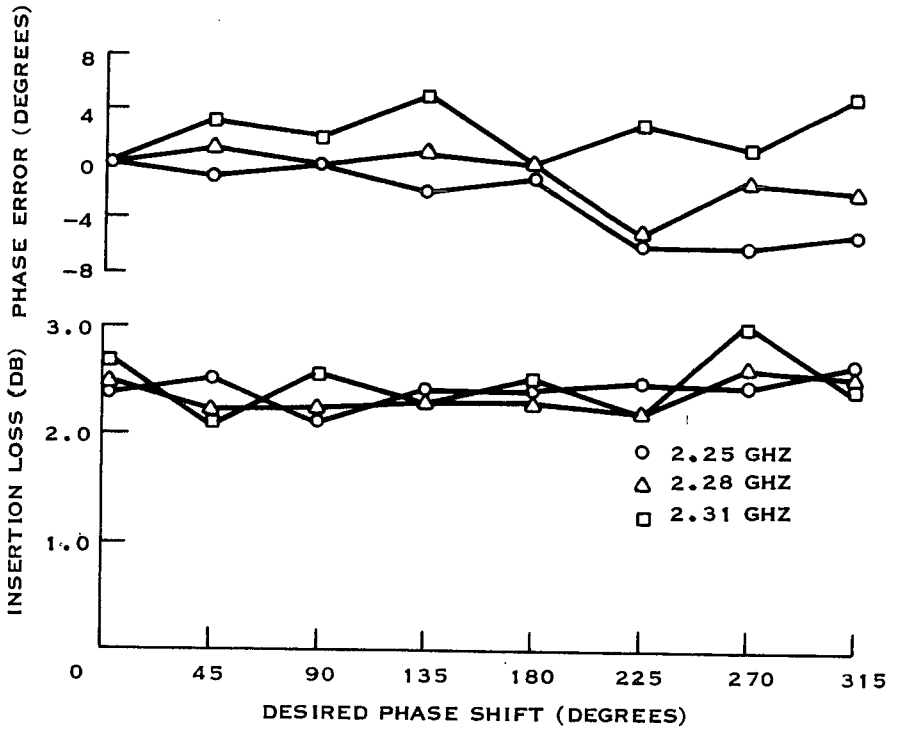


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Figure 3-52. Transmitter Phase Shifter Characteristics

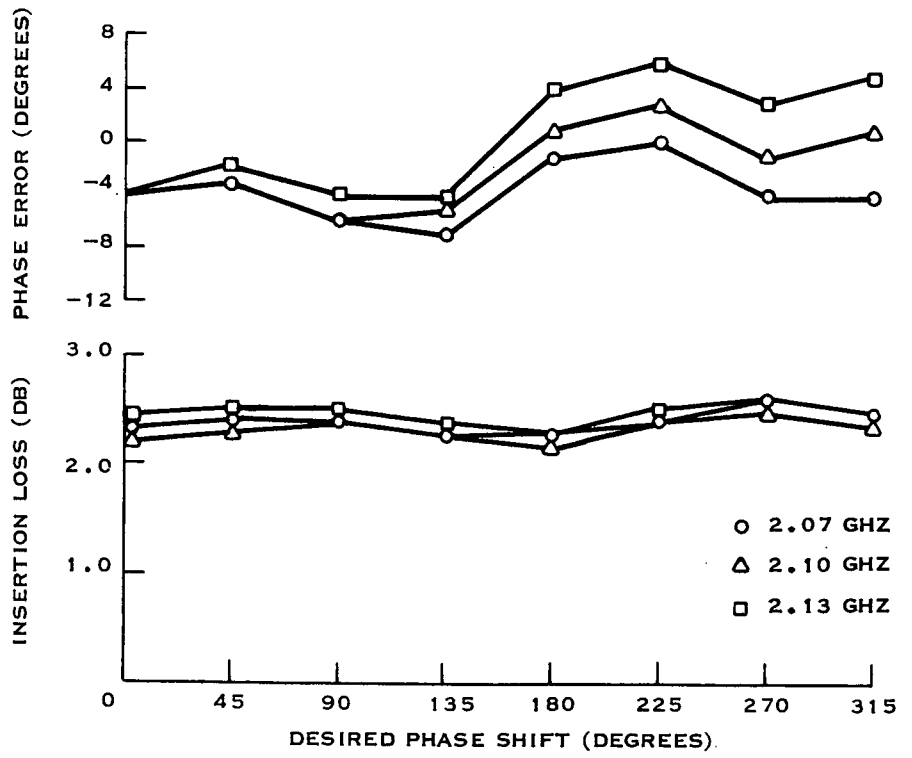

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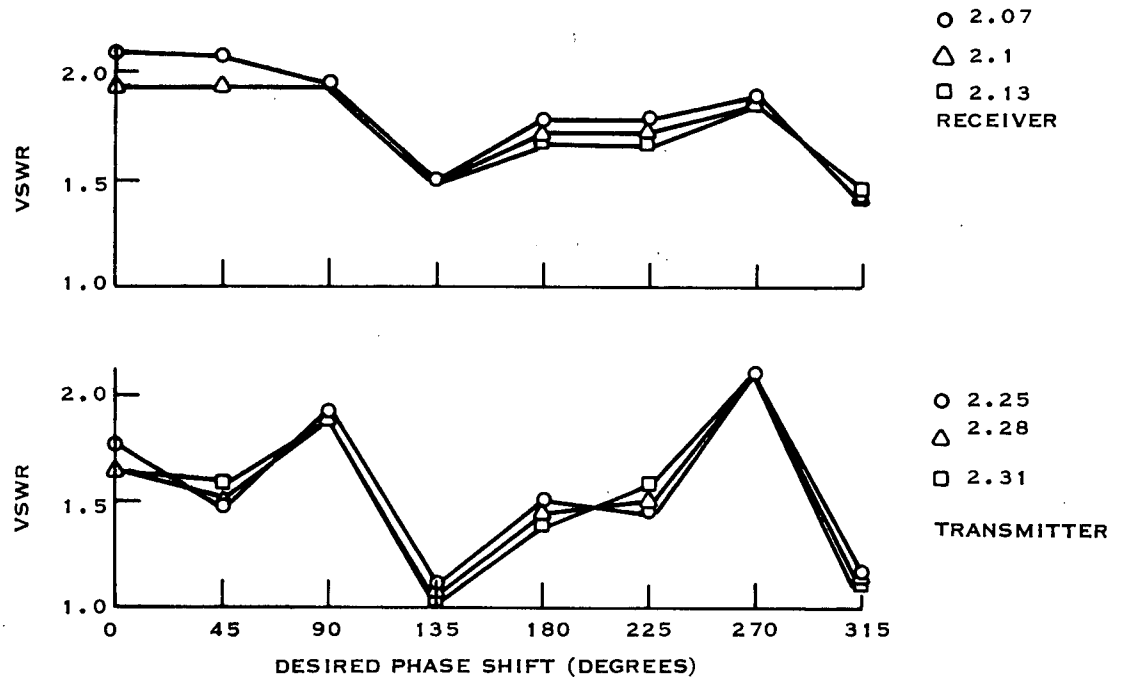
Figure 3-53. Receiver Phase Shifter Characteristics



149631

Figure 3-54. Phase Shifters Input VSWR

(b) Transmitter Amplifier

The transmitter amplifier gain and efficiency versus frequency is shown in Figure 3-55. These results were obtained with the input power held constant at 12 mW. The maximum output was approximately 1.5 watts. The indicated gain (approximately 21 dB) falls short of the design goal (24 dB) by 3 dB. This is the result of gain compression in the first stage of the amplifier.

The output spectrum of this amplifier was examined from 150 MHz to 22 GHz. The only spurious outputs observed were harmonically related to the input. These signals and their relative amplitudes are listed in Table 3-14.

TABLE 3-14. SPURIOUS OUTPUTS AND THEIR RELATIVE AMPLITUDES

Input Frequency (GHz)	Second Harmonic	Third Harmonic	Fourth Harmonic
2.25	−35 dB	−46 dB	<−50 dB
2.28	−32 dB	−32 dB	<−50 dB
2.31	−29 dB	<−50 dB	<−50 dB

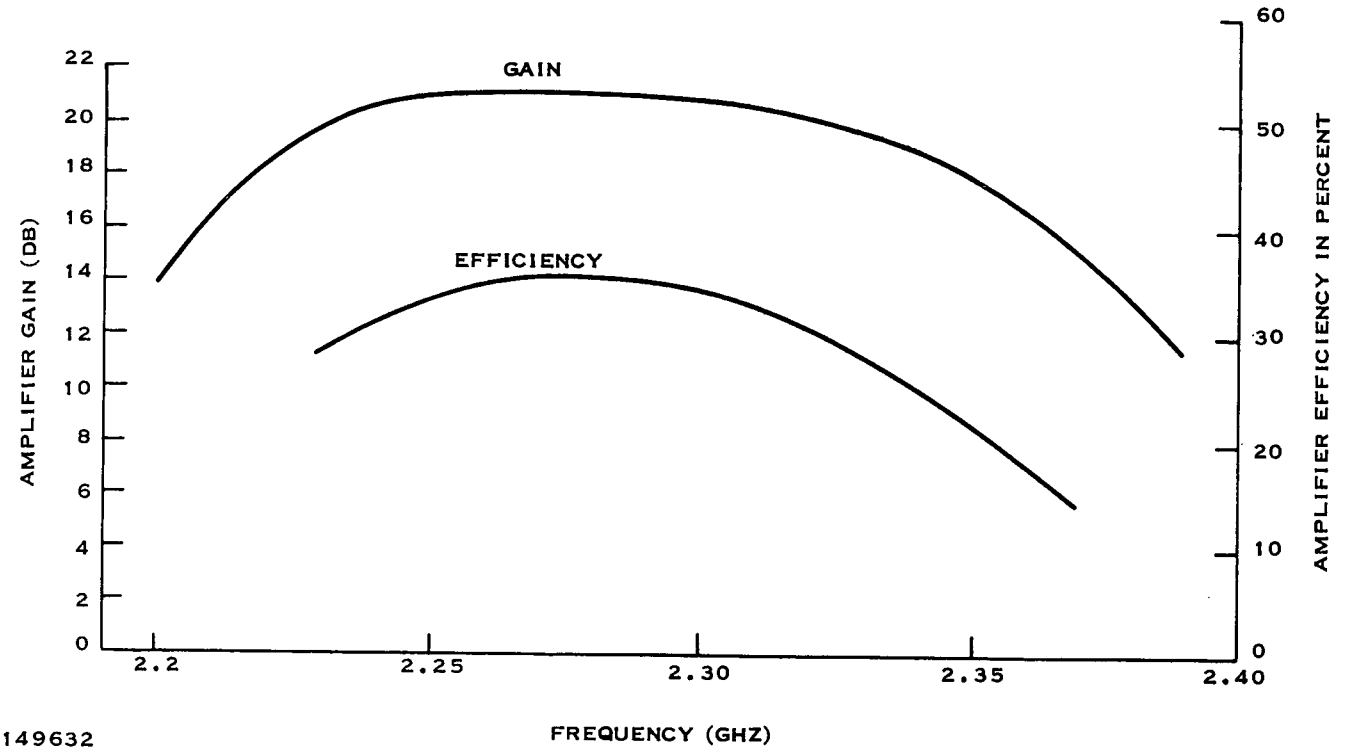


Figure 3-55. Transmitter Amplifier Gain and Efficiency Versus Frequency

(c) Low-Noise Amplifier

The low-noise amplifier gain response is shown in Figure 3-56. This curve indicates an in-band gain of 27.5 ±0.25 dB. Figure 3-57 gives the input VSWR and noise figure versus frequency. The relatively high VSWR is a result of mismatching the input for minimum noise figure.

(d) Transmitter Filter

Transmitter filter response is shown in Figure 3-58. The insertion loss in the transmit band varies between 0.5 and 0.3 dB. The loss in the receive band varies between 20 and 26 dB.

(e) Receiver Filter

Receiver filter characteristics are shown in Figure 3-59. The insertion loss in the receive band varies between approximately 0.8 to 1.1 dB, and 34 to 49 dB in the transmit band. The receive band VSWR varies between 1.1:1 to 1.5:1 and is greater than 12:1 in the transmit band.

(f) Diplexer

The diplexer characteristics are listed in Figure 3-60. Insertion loss, isolation and VSWR are listed for 2.06, 2.20 and 2.32 GHz.

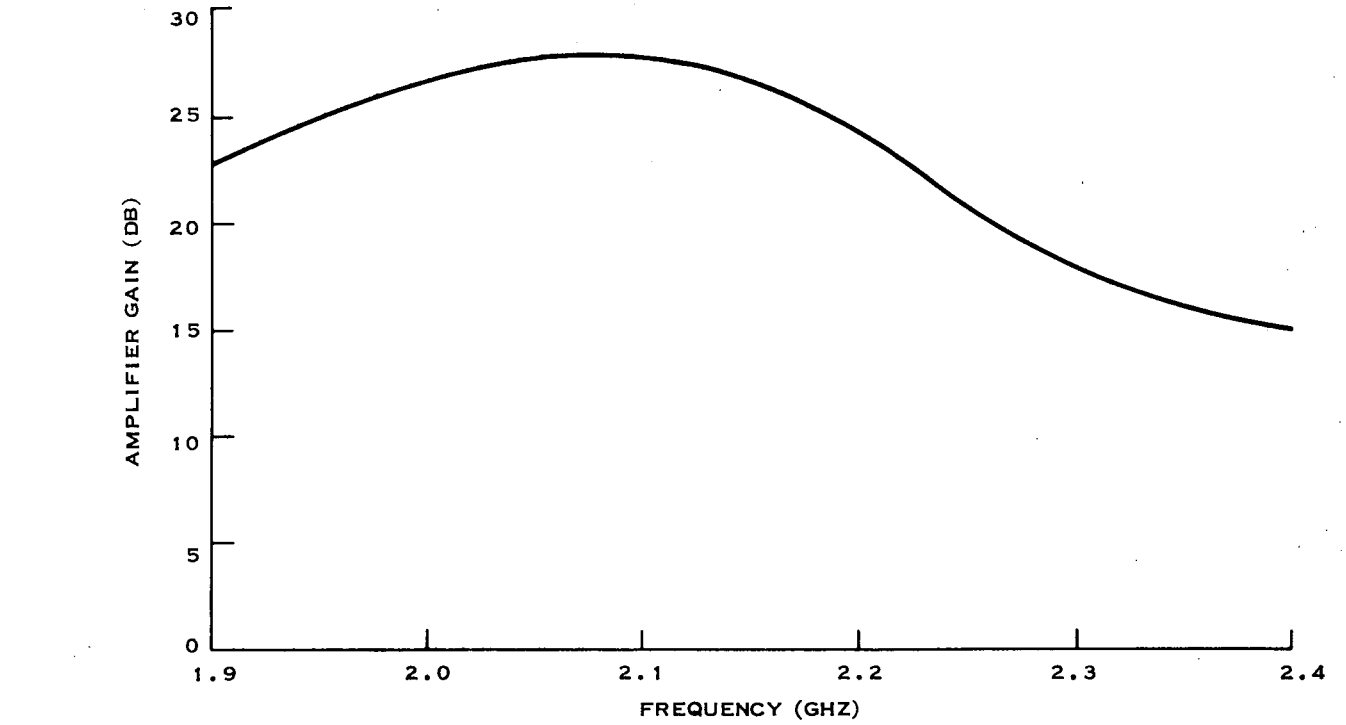


Figure 3-56. Low-Noise Amplifier Gain Versus Frequency

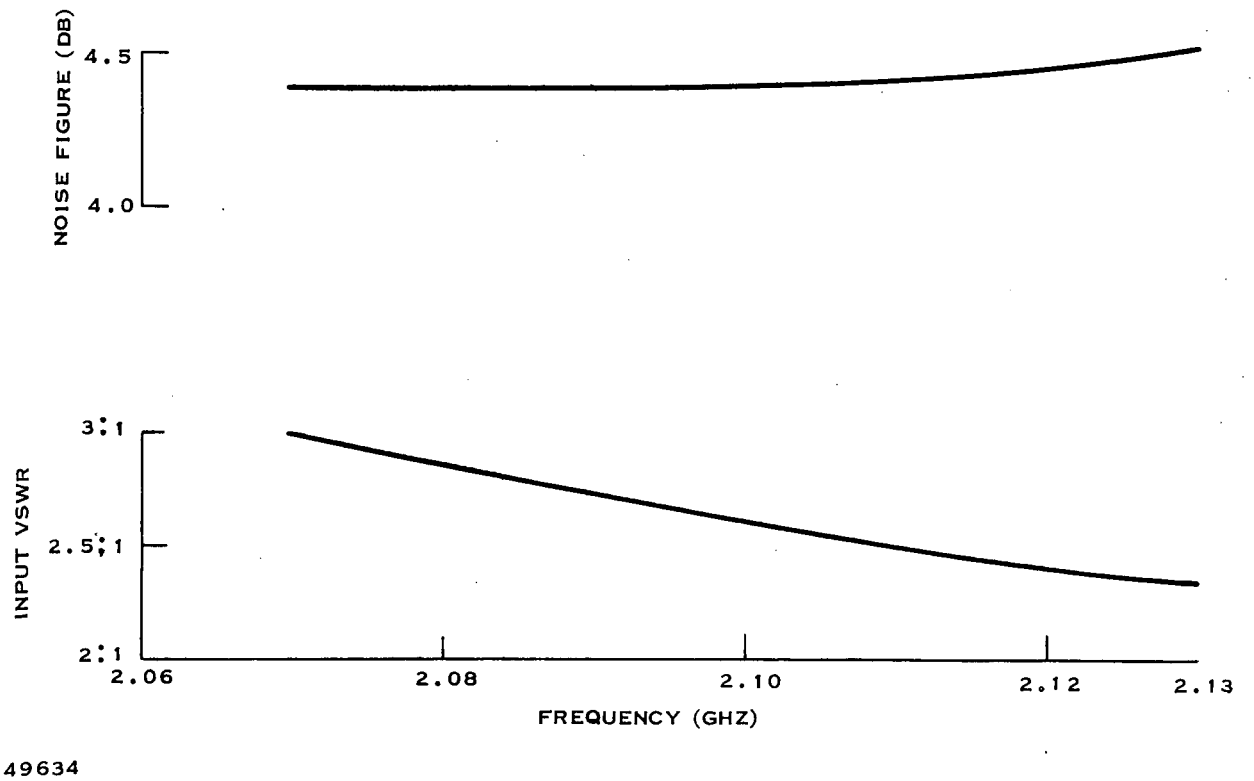


Figure 3-57. Low-Noise Amplifier VSWR and Noise Figure Versus Frequency

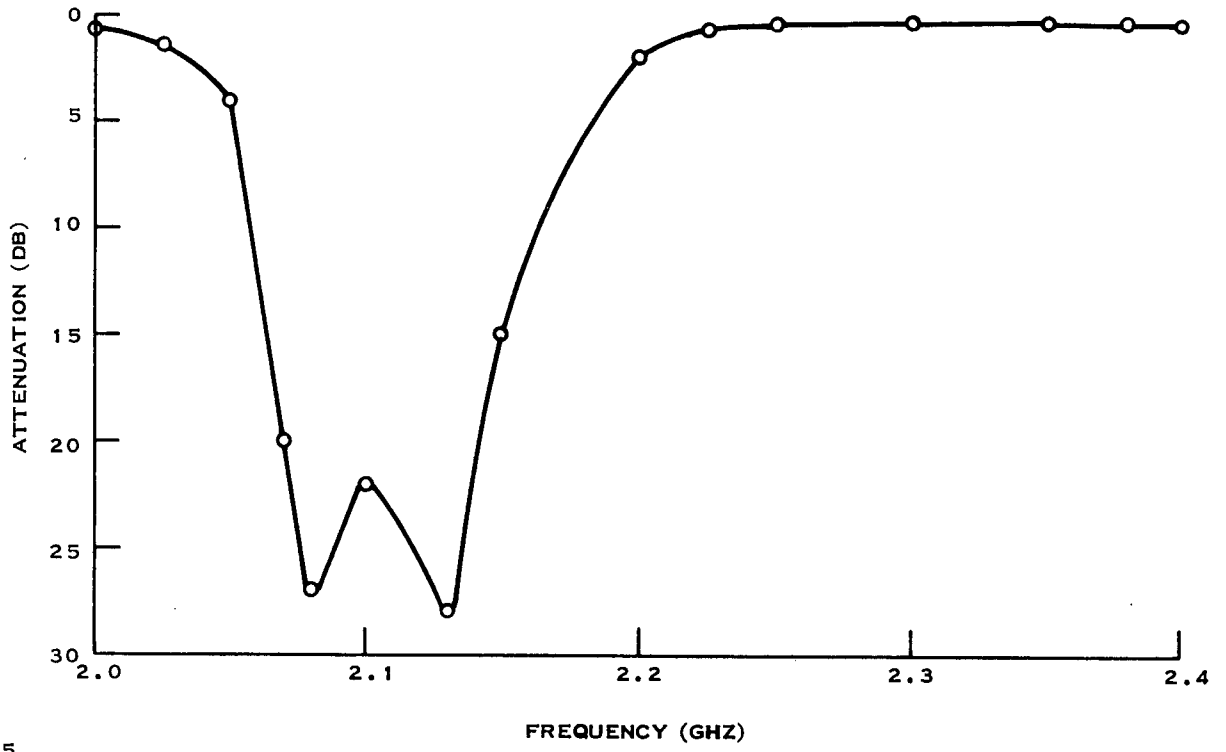


Figure 3-58. Transmitter Filter Attenuation Versus Frequency

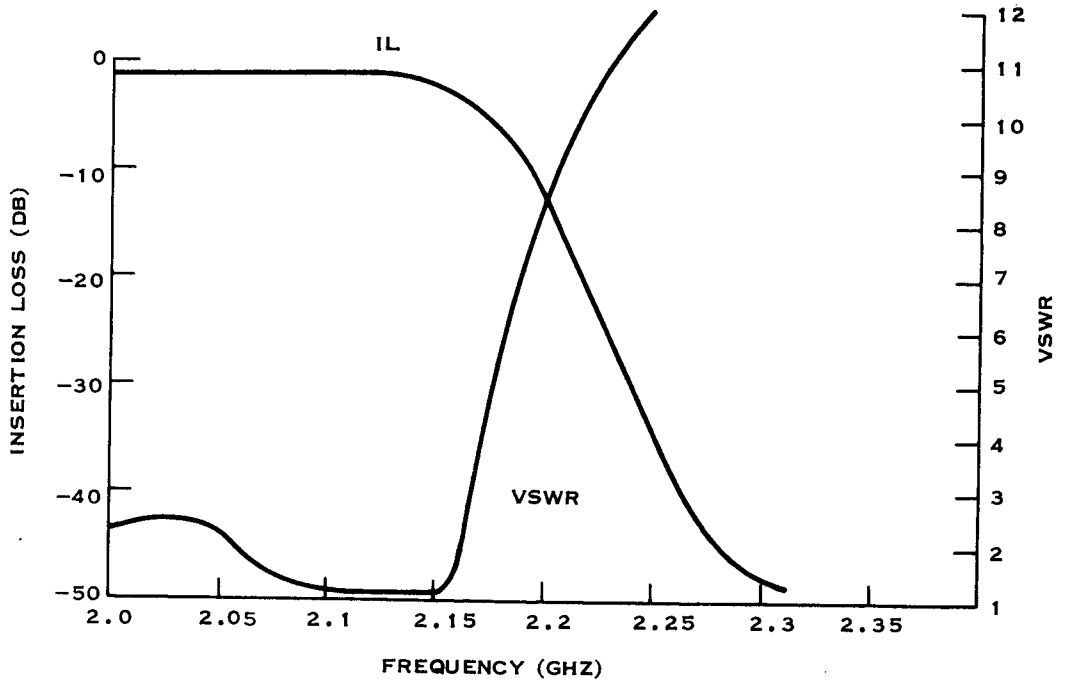
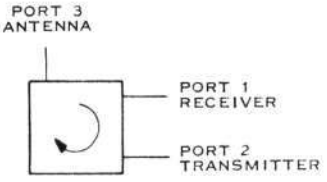


Figure 3-59. Receiver Filter Insertion Loss and Input VSWR



1	2	3	4	5	6	7	8	9	10
2.06	0.30	2.25	0.32	23	21	21	1.2	1.21	1.16
2.20	0.30	0.25	0.32	26	24	20.5	1.12	1.22	1.10
2.32	0.35	0.30	0.35	23	22	23	1.17	1.27	1.15

1 – FREQ (GHZ)
2 – 1 → 2 LOSS (DB)
3 – 2 → 3 LOSS (DB)
4 – 3 → 1 LOSS (DB)
5 – 2 → 1 ISOLATION (DB)
6 – 3 → 2 ISOLATION (DB)
7 – 1 → 3 ISOLATION (DB)
8 – PORT 1 VSWR
9 – PORT 2 VSWR
10 – PORT 3 VSWR

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Figure 3-60. Diplexer Data

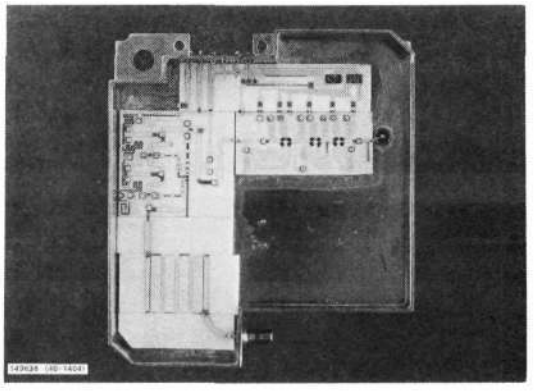

Figure 3-61. Module Receiver

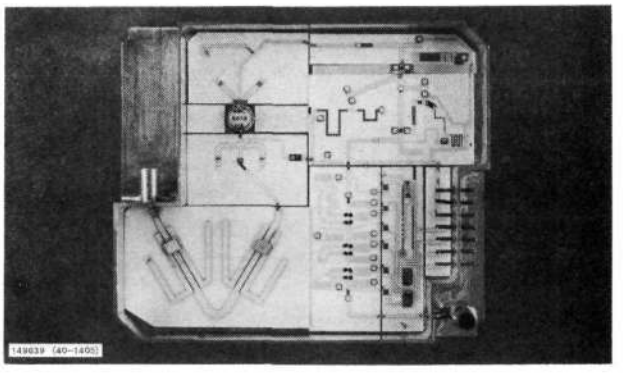

Figure 3-62. Module Transmitter

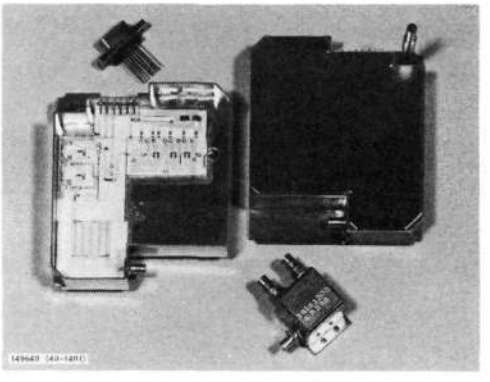

Figure 3-63. Module

(2) Module

The module test results are presented as transmitter and receiver test results. All tests were performed with the diplexer installed and the module fully assembled. During the module tests, only the portion of the module under test was energized. The receiver side of the module is shown in Figure 3-61, the transmitter side in Figure 3-62 and the complete module in Figure 3-63. The transmitter and receiver test data follows.

(a) Transmitter

Transmitter gain and efficiency versus frequency is shown in Figure 3-64. This test was performed with the input power held constant at 14 mW. The in-band gain, 19.5 ±0.35 dB, is slightly higher than might be expected, considering the gain of the amplifier. This higher gain reflects a lower input level at the amplifier which reduces the amount of gain compression in the first amplifier stage. Figure 3-65 shows phase-shift error and gain variation as a function of desired phase shift for 2.25, 2.28, and 2.31 GHz. The rms

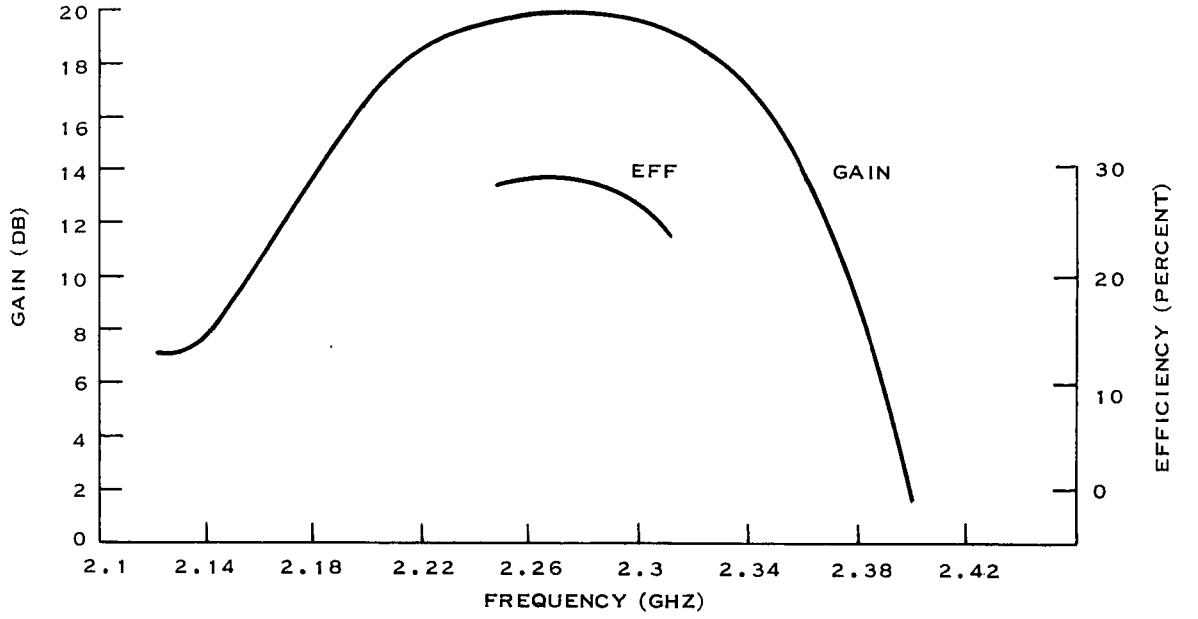

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Figure 3-64. Transmitter Chain Gain and Efficiency

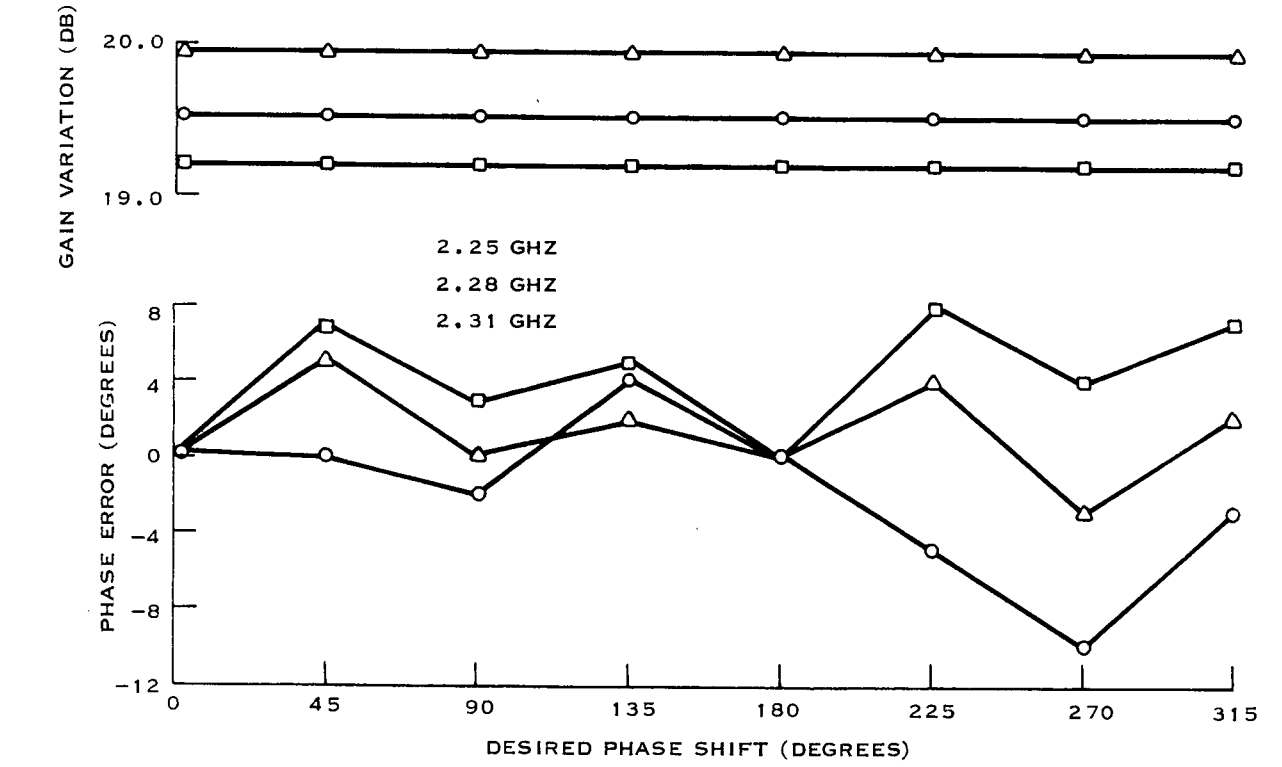

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Figure 3-65. Transmitter Phase Error and Gain Variation as a Function of Bit Position

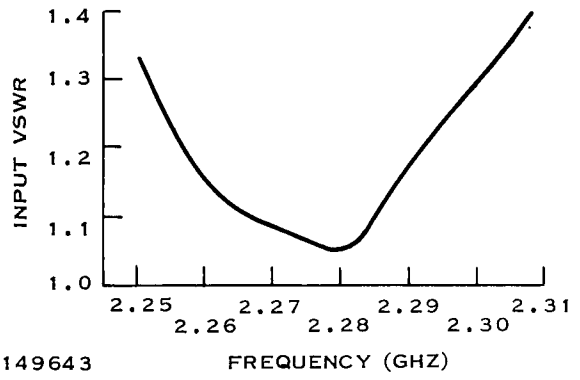

Figure 3-66. Transmitter Input VSWR in Reference to Bit Position

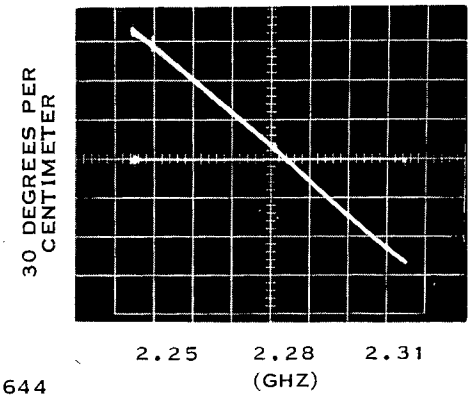

Figure 3-67. Transmitter Phase Linearity

phase-shift error, as computed from the peak errors, are 4.4, 2.7 and 5.2 degrees for 2.25, 2.28 and 2.31 GHz, respectively. The transmitter input VSWR versus frequency is shown in Figure 3-66. This test was performed with the phase shifter in reference position. Transmitter phase linearity is shown in Figure 3-67. This curve indicates a deviation from linear of approximately 5 degrees.

(b) Receiver

Receiver gain versus frequency is shown in Figure 3-68. An expanded in-band gain is also shown in this figure. The phase-shift errors and gain as a function of desired shift for 2.07, 2.10, and 2.13 GHz are shown in Figure 3-69. Using the peak phase shift errors, rms errors of 4.7, 3.4, and 5.5 degrees for 2.07, 2.10 and 2.13 GHz, respectively, were computed. Figure 3-70 gives receiver noise figure and input VSWR as a function of frequency. The noise figure varies from 5.5 to 5.9 dB with the transmitter off and 5.6 to 6.4 dB with the transmitter on. The input VSWR is a maximum of 1.72:1. Receiver phase linearity is shown in Figure 3-71. The horizontal line indicates the phase without the receiver and the inclined line with the receiver. The maximum deviation from linear appears to be approximately 3 degrees.

(c) Description of Tests

Tests were performed on the circuits and the module, essentially using four test-equipment arrangements. The following tests were performed using the equipment setup shown in Figure 3-72.

1. Phase-shift error and insertion loss as a function of desired shift (transmit and receiver phase shifters).
2. Low-noise amplifier gain.
3. Receiver filter response.
4. Transmit filter response.
5. Transmitter phase-shift errors.
6. Transmitter phase linearity.
7. Receiver gain.

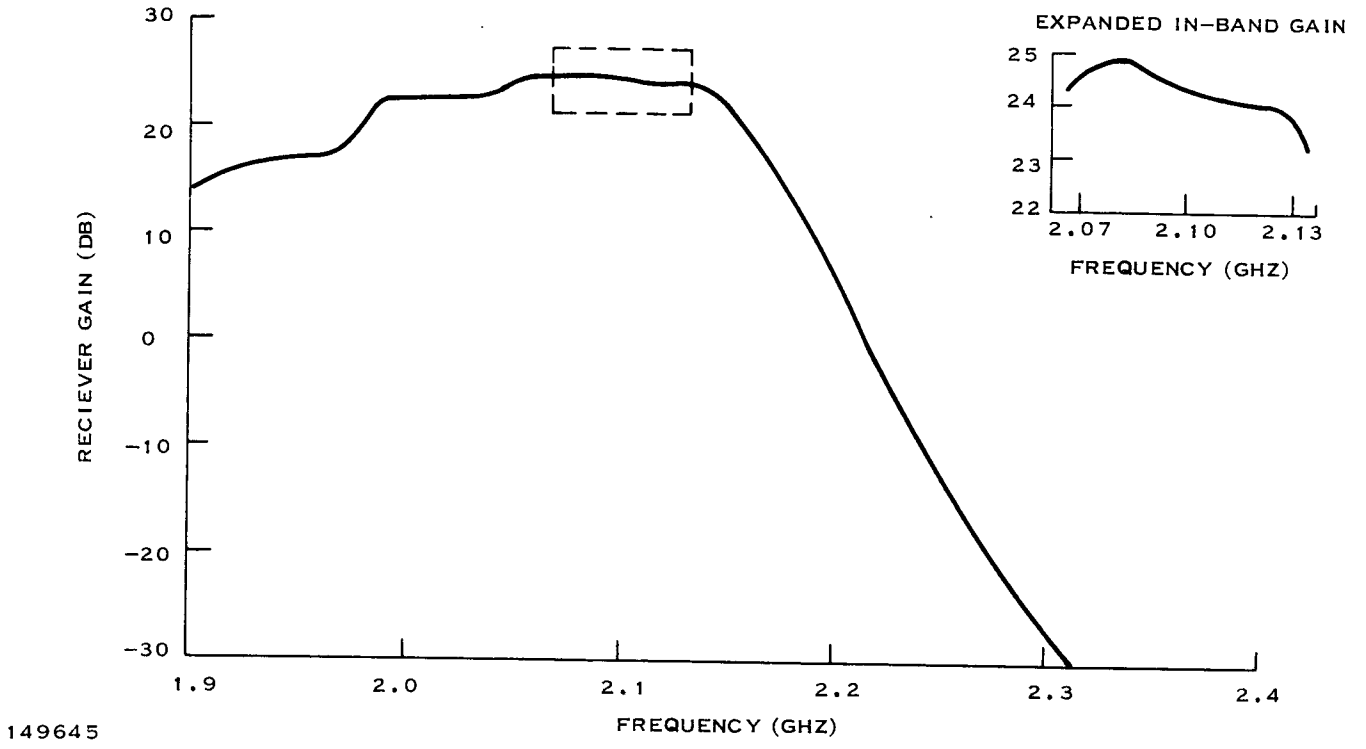

Figure 3-68. Receiver Gain

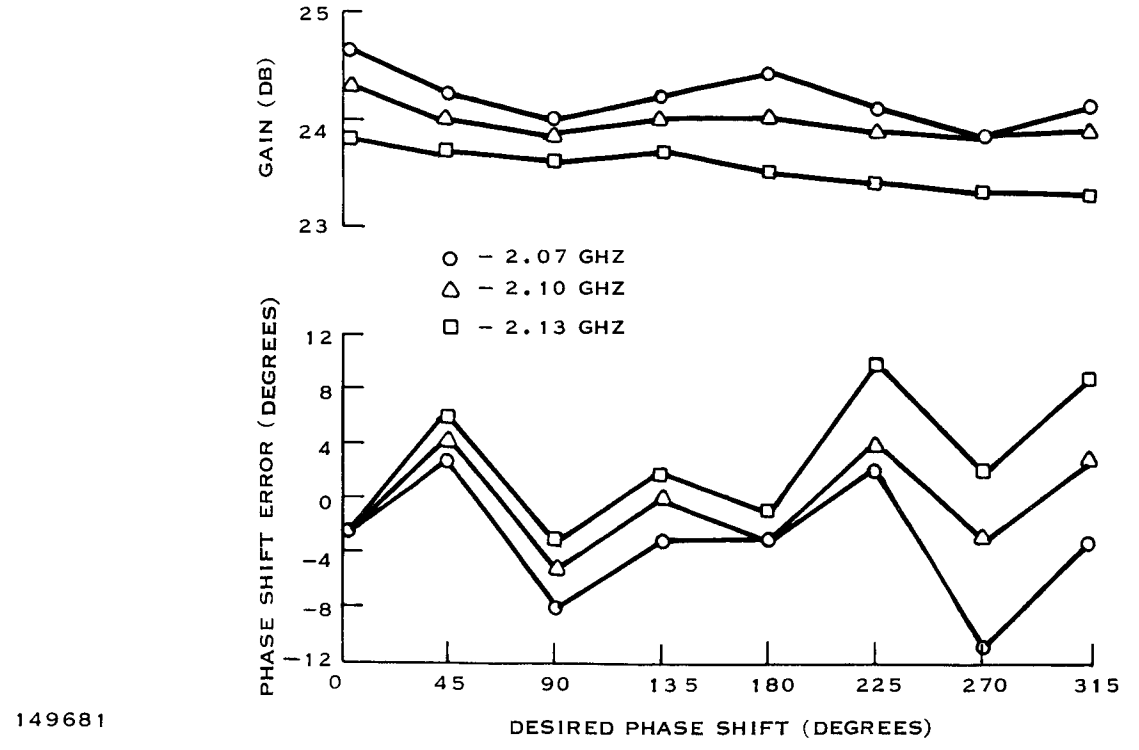

Figure 3-69. Receiver Gain and Phase Shift Error Versus Desired Phase Shift

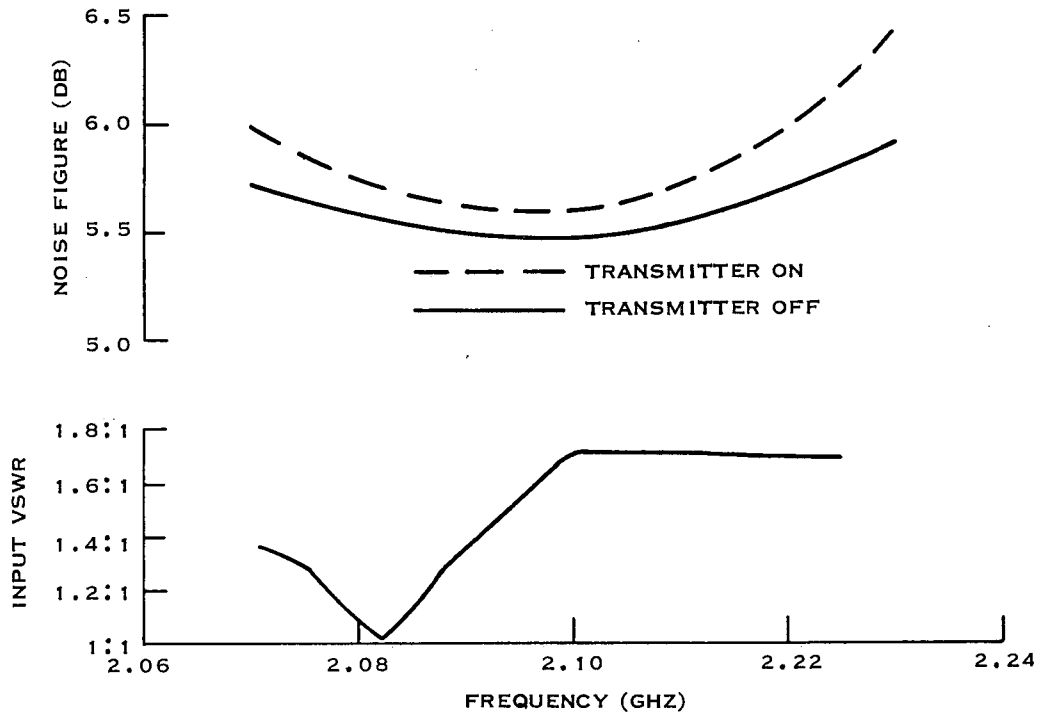

Figure 3-70. Low-Noise Amplifier Input VSWR and Noise Figure Versus Frequency

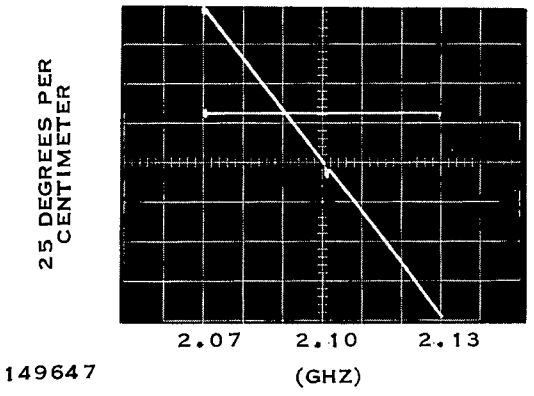

Figure 3-71. Receiver Phase Linearity

8. Receiver phase-shift errors.
9. Receiver phase linearity.

The following tests were performed using the equipment setup shown in Figure 3-73.

- Phase-shift input VSWR (receive and transmit phase shifters).
- Low-noise amplifier input VSWR.
- Receiver input VSWR.

Tests involving medium or high powers cannot easily be performed using the HP network analyzer. The following tests were performed using the equipment setup shown in Figure 3-74.

1. Power amplifier gain.
2. Power amplifier efficiency.
3. Transmitter gain.

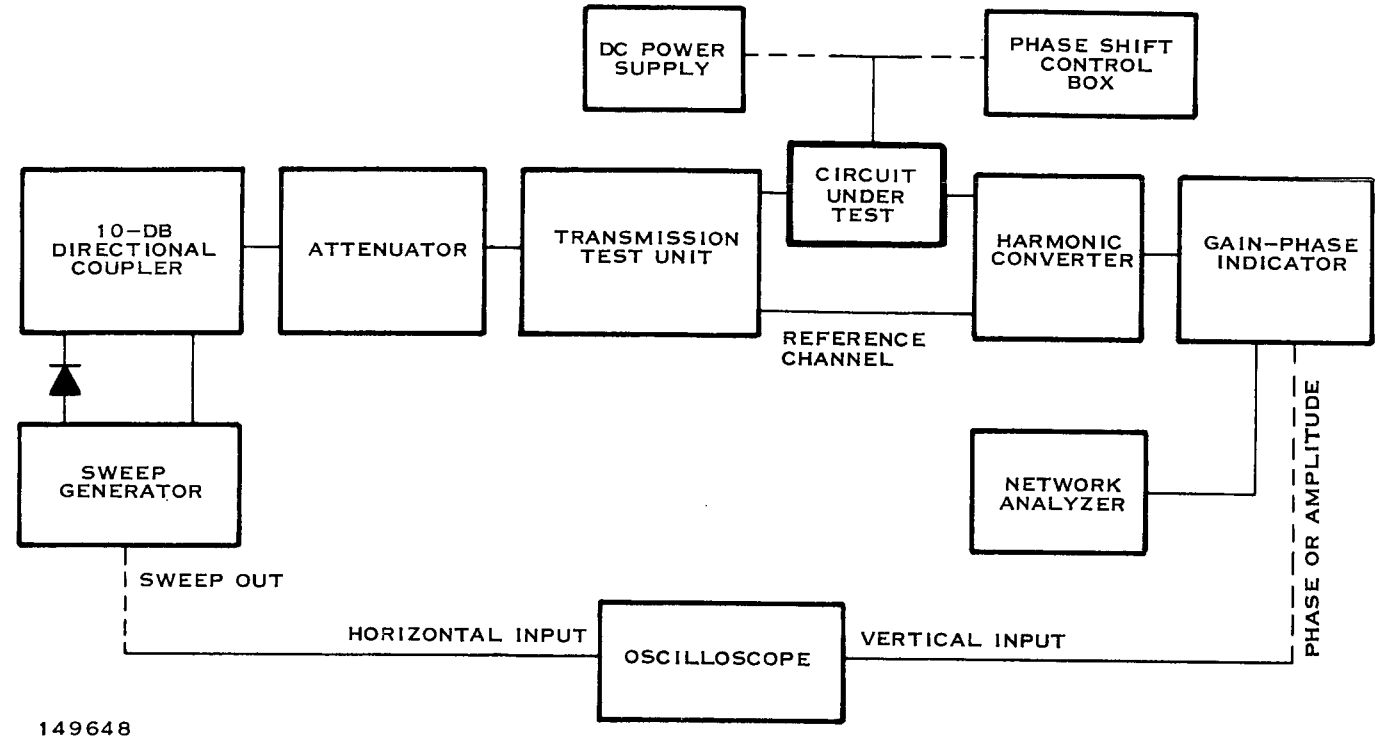

Figure 3-72. Amplitude and Phase Measurement Setup

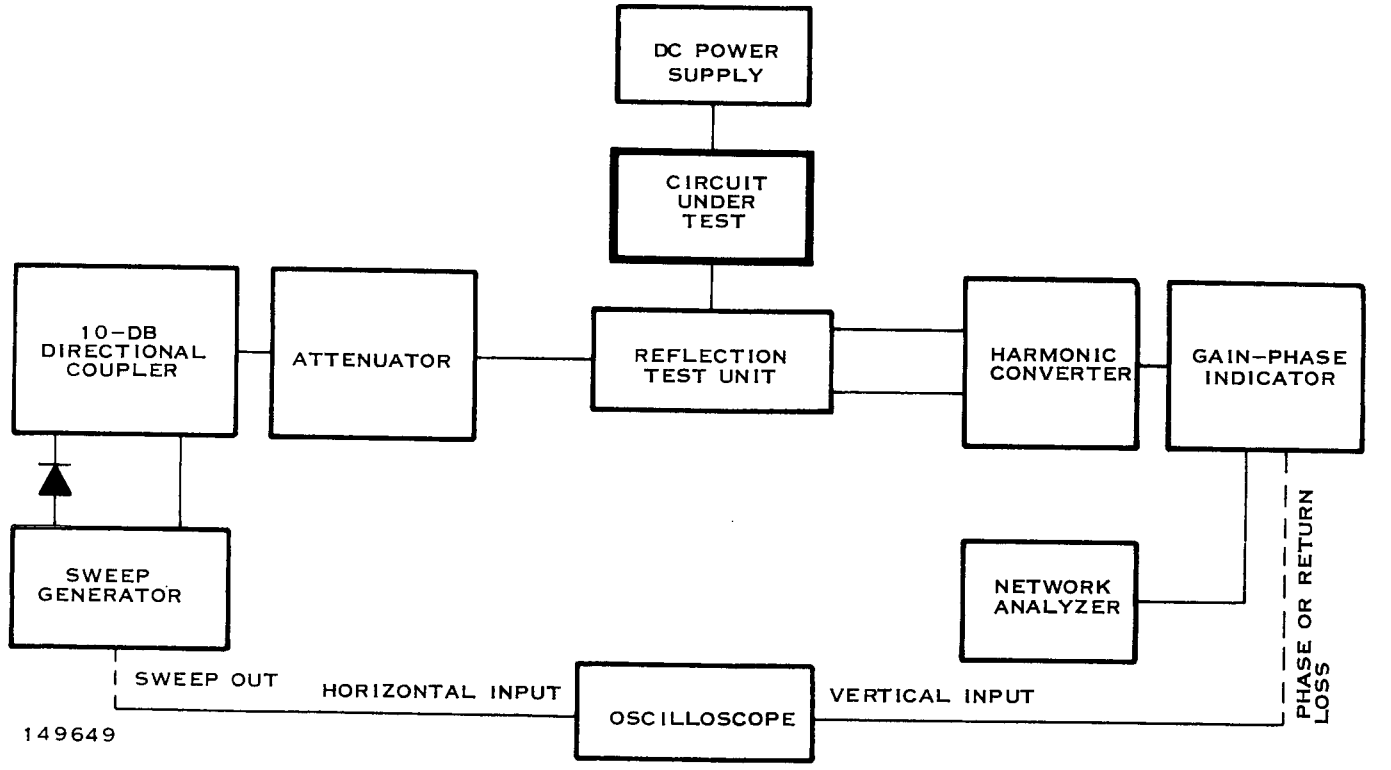

Figure 3-73. VSWR Measurement Setup

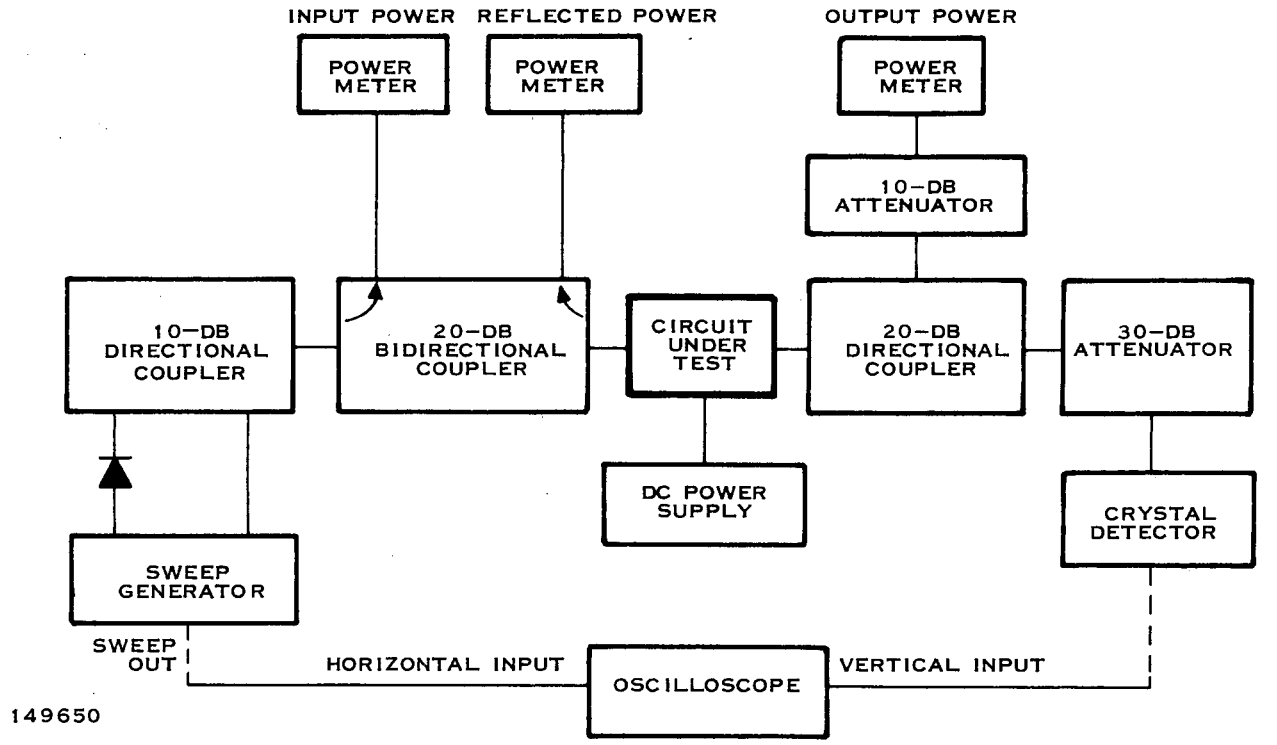

Figure 3-74. Power Gain and VSWR Measurement Setup

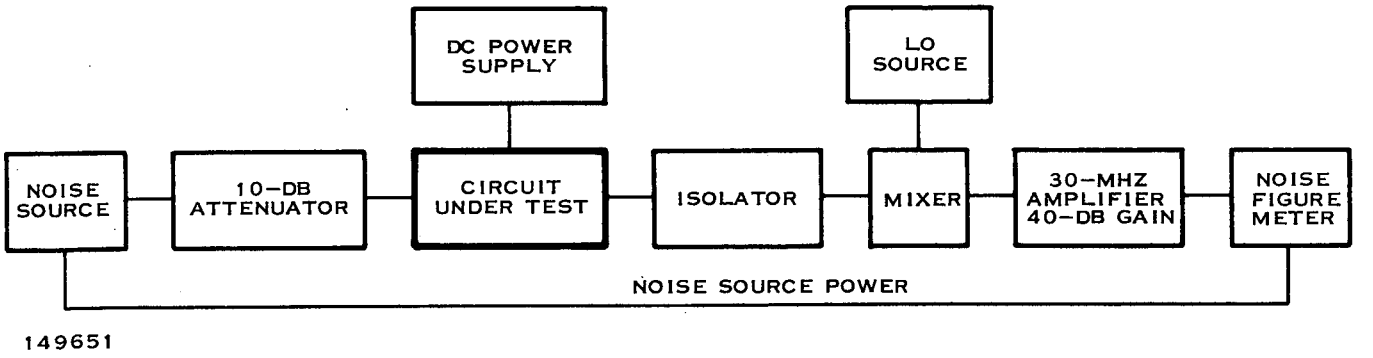

Figure 3-75. Noise Figure Measurement Setup

4. Transmitter efficiency.
5. Transmitter input VSWR.

Noise-figure measurements for the low-noise amplifier and the receiver were performed, using the equipment shown in Figure 3-75. Table 3-15, the module performance goals versus actual performance, is shown below.

TABLE 3-15. MODULE PERFORMANCE GOALS VERSUS ACTUAL PERFORMANCE

	Performance Goals	Actual Performance
Transmitter		
Output power	>1.0-W CW	>1.0-W CW
Gain	>22 dB	>19 dB
Input VSWR	<1.3:1	<2:1
Efficiency of power chain	>25 percent	>24 percent
Phase errors	<10 degrees (maximum)	<10 degrees (maximum)
	<5 degrees rms	<5.2 degrees rms
Phase linearity	±5 degrees (maximum)	<5 degrees (maximum)
Receiver		
Amplifier noise figure	<4.5 dB	4.5 dB
Gain	>23 dB	>24 dB
Transmitter frequency rejection	>40 dB	>35 dB
Phase errors	<5 degrees rms	<5 degrees rms
	<10 degrees (maximum)	<12 degrees (maximum)
Phase linearity	±5 degrees (maximum)	<3 degrees

4. Reliability

a. Introduction

For almost any component subsystem or system, the mean time to failure can be shown to be an experimental function of temperature. As a result, any stated mean time to failure assumes that the system has a fixed operating temperature which is at least known as a function of the ambient temperature in which it is operating. The prediction made in the Phase I Final Report was based on standard, well-accepted failure rates from the RADC handbook, and on a thermal design which allows the maximum semiconductor junction temperature to rise to 120°C. The exception was made that the microwave power transistor could have a junction temperature of 150°C due to its high-power dissipation and thermal impedance.

Further analytical investigation into failure rates was made to determine if those predictions made in the first phase final report were valid. It has been concluded that all failure rates determined in Phase I, with the exception of the medium-power transistor rate, were valid. A description of the investigation of the MTF for this transistor is given in the following paragraphs. Electromigration is a long-term failure mechanism in the metalization of semiconductor devices under high-current density, high-temperature conditions. The failure mode can be an open circuit caused by void formation within the metal film or it can be a short circuit between adjacent metal patterns caused by a buildup of metal (hillocks) or whisker growth. This mass transfer of metal is the result of collisions between conduction electrons and

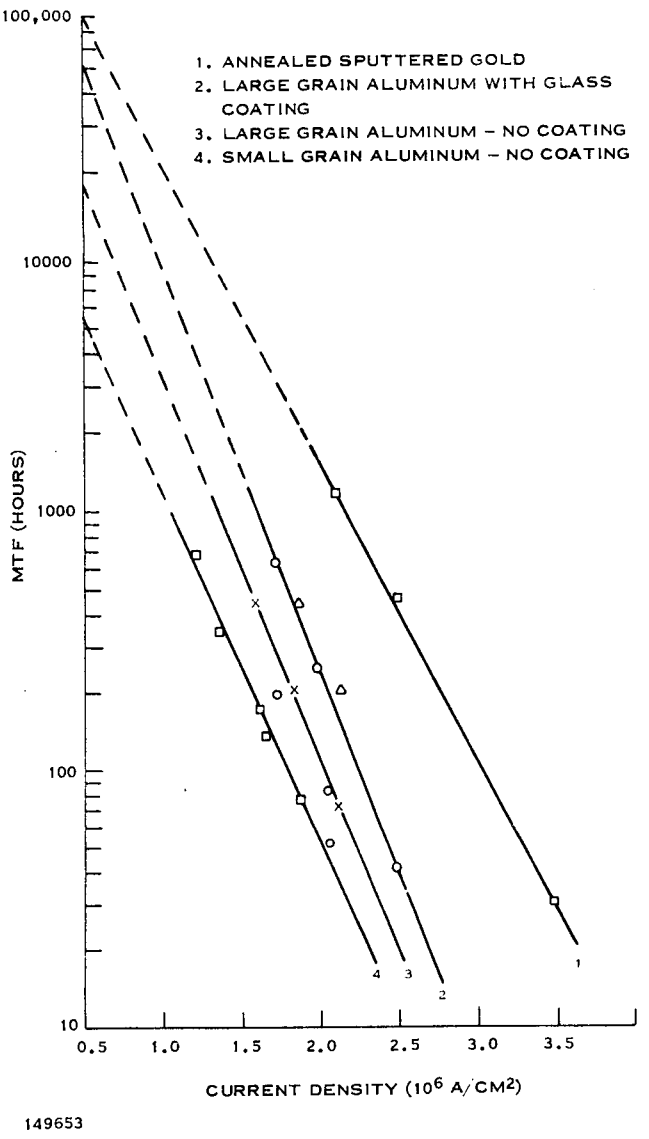

Figure 3-76. High-Current Stress in Aluminum and Sputtered Gold Films at 150° T_j (Corresponds to Operating Junction Temperature)

free metal ions and consequently, the metal ion movement is in the direction of electron flow. Thus, voids move toward the negative potential end while hillocks tend to form at the positive end of the metal film. The size of S-band transistors and their thermal impedance and therefore their junction temperature makes them particularly susceptible to failure from electromigration. Electromigration in metal films is a function of current density, film temperature, cross section area, film grain size, and surface passivation. Black[1] found empirically that the MTF of single aluminum films is given by the expression

$$MTF = C\frac{A \exp(\phi/kT)}{J^2}$$

where

C = experimental constant depending on film properties

A = Cross section area of metal film (cm^2)

ϕ = activation energy of metal film (eV)

k = Boltzmann constant

T = film temperature (°K)

J = current density (A/cm^2).

This expression shows that the MTF due to electromigration is inversely related to the square of current density, exponentially related to temperature (doubling for every 10°C decrease in temperature), and linear with cross section area. The constant C varies significantly, depending on film properties such as surface passivation, grain size, and the specific metal used. For example, Black shows that passivation of aluminum films with glass layers results in a 10 to 20 times improvement in MTF for typical device operating conditions, while the improvement from small to large grain aluminum also is on the order of 10 to 20 times.

IBM has reported the relationships between MTF and lengths and widths of the resistors stripes.[2] Texas Instruments has taken data on 50-mil long stripe geometry and, according to the IBM relationships, is on the conservative side. IBM has shown that MTF increases for narrower and shorter stripes which are employed on the MSC transistors. Microwave transistors have smaller geometries, however, and the MTF for leads in these transistors is greater than the estimated value. All of the above discussion assumes that the current is dc.

Migration tests reported in reference (2) have shown the MTF for ac to be typically 100 times greater than for dc for densities up to 10^7 A/cm^2. In fact, theory predicts that no migration occurs for pure ac. Experiments confirm that simply reversing polarities can cause hillocks to refill voids. In normal amplifier applications however, currents are not pure ac but have dc components.

Microwave devices such as the MSC 3005 have been operating in communication amplifiers in the field for up to a year without failure due to electromigration. Thus, it appears that the estimates of failure rate (Figure 3-77) given by the MSC 3005 manufacturer (160,000 hours) are justified.[3] MSC is currently developing gold-metalized transistors which may give enhanced lifetimes. Manufacturers must be extremely careful that a significant process change such as conversion to new metal systems leads to a significant improvement in migration MTF under actual RF conditions and does not introduce new or unforeseen problems which may be as severe as the original problem. To this point, the amount of knowledge of gold-metalized devices is relatively limited in comparison to the years of data acquired on aluminum metalization. Gold has been proposed as an alternate to aluminum for improved migration MTF, based on its higher activation energy. The diffusion constant of gold has a greater temperature dependence than aluminum and Black's original derivation does not take into account the temperature gradients and structural inhomogeneities present in the leads. Since Black's first derivation, more is known about the failure mechanisms in aluminum films subjected to HCS. The current thinking is that

$$\text{MTF} = A\, J^{-n} \exp(\phi/kT)$$

where $2 < n < 3$.

IBM has published extensive data on electromigration in aluminum film conductors. According to Rosenberg and his coworkers[4]

$$\phi = 0.51 \text{ eV for a 1 } \mu\text{m grain size Al film}$$

and

$$\phi = 0.73 \text{ eV for a large grain size (5 to 8 } \mu\text{m) Al film}$$

and that glass passivation does not increase the activation energy to 1.2 eV as suggested by Black.

It is generally agreed that electromigration in Al films is surface (grain boundary) diffusion controlled and that the activation energy for surface (grain boundary) diffusion should be pertinent to electromigration data. For metals, the activation energy for surface diffusion is approximately one half of the activation energy for self diffusion in bulk ($\sim$1.4 eV). It is concluded that Rosenberg's value, $\phi = 0.73$, is more reliable. Even though no experiments to determine ϕ have been made, Texas Instruments internal data is consistent with $\phi = 0.73$ eV, or less. There is no indication in other industrial laboratories, except for the work of Black that $\phi = 1.2$ eV.

In early 1972, an unpublished study on electromigration was made by the Texas Instruments Antenna & Microwave Systems Department. The results were extrapolated to 150°C (Figure 3-76) for bulk material gold and aluminum metalizations.

It may be concluded that gold is superior to aluminum in so far as this failure mechanism is concerned. The correct density for the proposed transistor is roughly 5×10^5

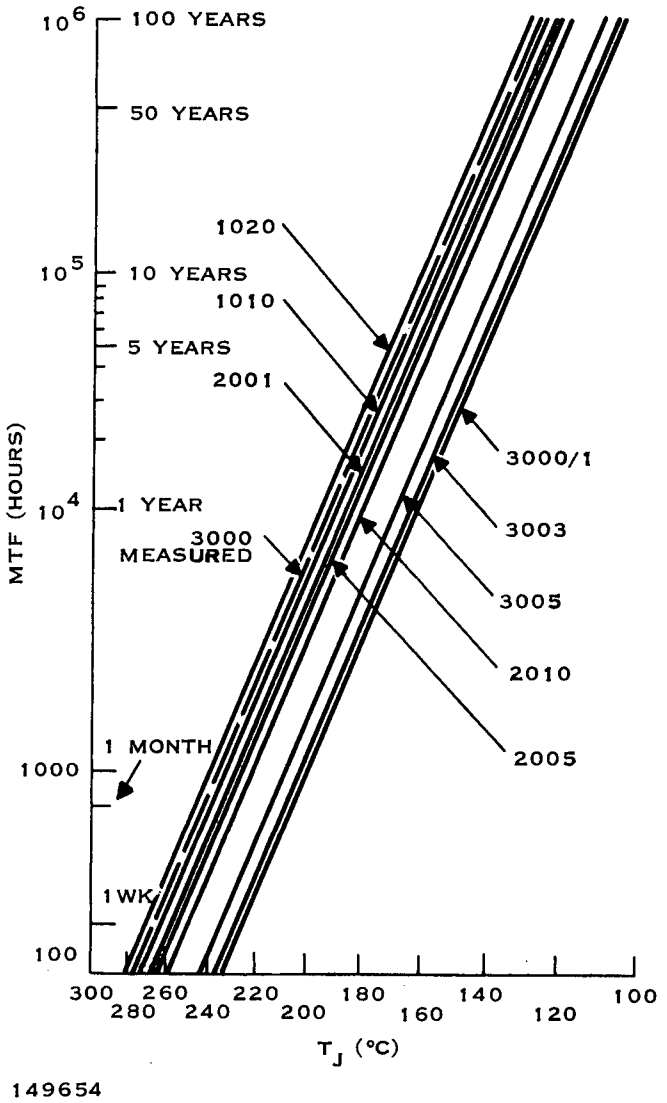

Figure 3-77. Measured and Calculated Migration MTF of MSC 1000, MSC 2000, and MSC 3000 Series

A/cm^2 so that a 55,000-hour MTF may be expected and, consequently, could have a lower MTF than aluminum due to thermal gradients present in any device, as a result of thermal migration. The general phenomenon of metal migration can occur in any system having nonhomogeneous regions with the resultant differences in metal ion mobilities. This differential mobility can also be produced by thermal gradients. The phenomenon of migration observed in operating transistors is most likely due to a combination of electromigration and thermal migration. This point must be considered since many of the tests showing gold to have an improved resistance to migration were run under uniform temperature conditions and thus, do not include thermal migration. Thus, the real test is to evaluate gold migration in actual RF conditions.

TRW recently announced a family of gold-metalization transistors with a low thermal impedance (2.5°C/W) and a lower operating temperature than the MSC devices. Reportedly, it is in production for a military program. Tests under actual RF conditions will consequently be made soon.

A currently realistic failure rate for this component should be $6.25/10^6$ hours. Appendix E of the first phase study is modified and is included as Appendix B of this report. The allowable number of transmit failures without declaring the array failed remains at 64. The conclusion is reached that the overall system survival probability is changed little even with the increased failure rate.

b. Experimental Results

The module case contained deficiencies which prevented an adequate seal. To have obtained a complete seal would have meant the application of excessive heat which would damage the substrates. A new case was designed and will be used for future modules.

5. Recommendations

Module performance may be improved with work in the following areas, including the phase shifters, the transmitter amplifier, the receiver filter, and the receiver amplifier.

The phase shifter performance can be improved by a more careful circuit layout. The insertion loss and input VSWR variation as a function of bit position (Figures 3-52, 3-53, 3-54) indicates a need to optimize the diode bias lines. These are the quarter-wavelength lines which are shunted across the main transmission line. These lines were meandered too closely and this effectively reduces their electrical lengths. This problem can be corrected by another layout and, possibly, by an increase in the size of the circuit.

The receiver filter needs to be optimized to provide a full 40-dB attenuation over the transmit band. The present filter provides only 34 dB at the low end of the transmit band. This problem can be corrected by further work on the filter or by going to an eight-element filter of the same type.

Since the low-noise amplifier was designed, new transistors have been developed which could reduce the noise figure by 1 dB. An amplifier noise figure of approximately 3.4 dB and a module noise figure between 4.5 and 5.0 dB would result. Incorporating the new transistor in the module receiver at most would require the redesign of the first stage of the low-noise amplifier. It is possible, however, that the two transistors are completely interchangeable.

The first stage of the transmitter amplifier operates in gain compression from 2 to 3 dB. To eliminate this, a higher power transistor will be required in the first stage. The redesign of this stage will be required. In the present module, however, this condition buffers amplitude changes in the phase shifter.

REFERENCES

1. J.R. Black, *IEEE Transactions,* ED-16, p 338 (1969).
2. B.N. Agarwala, M.J. Attardo and A.P. Ingraham, *Journal of Applied Physics,* Vol. 41, p 3594 (1970).
3. Walter E. Poole, "Electro-Migration in Microwave Power Transistors," unpublished report.
4. M.J. Attardo and R. Rosenberg, *Journal of Applied Physics,* Volume 41, p 2381, 1970).

SECTION IV
RECOMMENDATIONS FOR FUTURE WORK

The AESPA system block diagram is shown in Figure 4-1. The approach taken to demonstrate system feasibility was to develop those system components containing the greatest technical risk. As a result, the array and supporting structure and the electronics module were developed first. The transmit manifold was developed out of necessity to prove the array performance.

Priority for future work falls into two categories; improvements to system components developed during this phase of the contract and development of other system components and studies not covered in this second phase.

A. Order of Priority

System components developed during the second phase require the following improvements:

- Reduce module weight
- Reduce module noise-figure
- Incorporate Phase Trim in each module
- Increase transmitter efficiency
- Increase transmitter reliability
- Improve antenna manifold.

Module weight reduction improvements can be achieved only through adherence to a strict weight-reduction program. Transmitter/receiver reliability can be enhanced by incorporating new devices in other modules. Phase trim can be incorporated in other modules by using variable-length RF line, or by digital correction. A combination of these is the approach recommended.

B. Reliability Development

Reliability development work must be concluded satisfactorily. The original proposal and the first phase report indicate that the failure rates for medium power (1-watt) S-band transistors are similar to those for lower frequency devices but current devices have higher failure rates. Since this transistor has the highest failure rate in the system, efforts should be made to monitor transistor developments to select a device which has the lowest failure rate, and to reduce the junction temperature, thereby reducing failure rate. The module case must be redesigned to permit a hermetic seal so that a full series of environmental tests may be run.

C. Antenna Manifold Improvements Program

Needed antenna manifold improvements include the areas of materials and electrical performance. Although the manifold exhibited excellent resilience and low weight, other programs have not had the same unqualified success with PPO material. Future work must

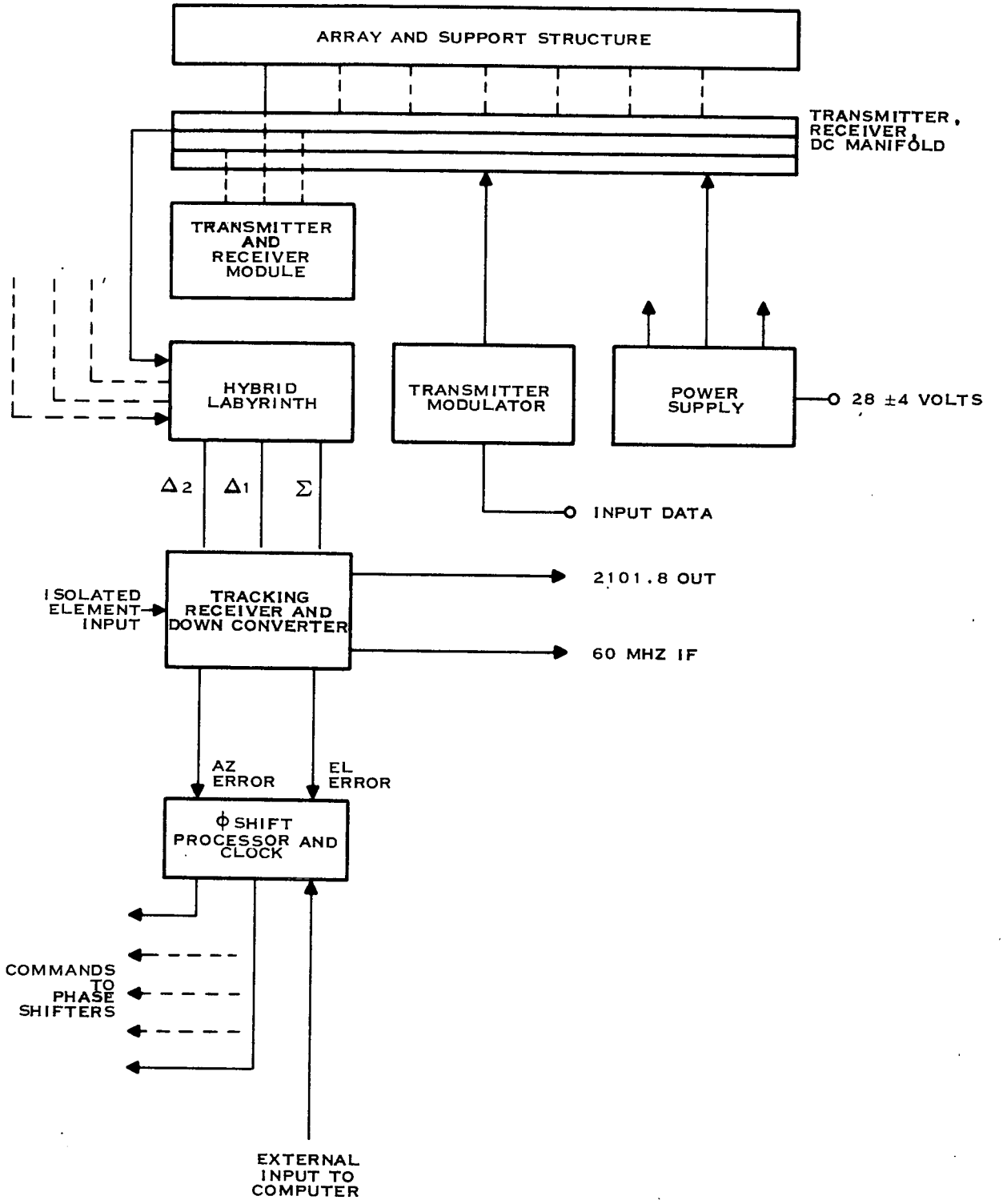

Figure 4-1. AESPA System Block Diagram

include an in-depth look at manifold materials, particularly with reference to weight. Measurements on the array with the element placement raised with respect to the ground plane should be made to enhance the aperture efficiency.

Electrical performance priorities include

- Development of the beam-steering logic
- Development of additional modules to fill the array
- Development of receive and logic manifolds to operate the modules in the array
- Development of a microwave integrated-circuit tracking receiver
- Development of the modulator/transmitter.

D. Program for Future Work

With these priorities established, the following program is recommended

1. Development of the beam-steering logic
2. Construction of 12 additional modules incorporating phase trim and lower noise figure and capable of being hermetically sealed.
3. Development of an RF receive manifold and a logic manifold.

APPENDIX A
ARRAY PATTERNS

To present the basic measurements of the 128-element antenna in a not too lengthy description of the text of this report, many of the antenna patterns have been placed in this appendix for clarity and completeness.

The patterns may be classified as follows:

1. Additional patterns at 2282 MHz
   a. Patterns using LHCP source
      (1) Σ Elevation—60 degrees per cycle (Figure A-1)
      (2) Σ & Δ Azimuth—60 degrees per cycle (Figure A-2)
   b. Patterns using rotating horn
      (1) Patterns at 360 degrees per cycle scale
         (a) Center element—azimuth (Figure A-3)
         (b) Σ Elevation (Figure A-4)
         (c) Σ & Δ Azimuth (Figure A-5)
         (d) Σ & Δ Azimuth—30 degrees scan (Figure A-6)
         (e) Σ & Δ Azimuth—60 degrees scan (Figure A-7)
      (2) Patterns at 60 degrees per cycle scale
         (a) Σ Elevation (Figure A-8)
         (b) Σ & Δ Azimuth (Figure A-9)
2. Patterns at 2101 MHz
   a. Patterns using LHCP source
      (1) Patterns at 360 degrees per cycle scale
         (a) Σ Elevation (Figure A-10)
         (b) Σ & Δ Azimuth (Figure A-11)
         (c) Σ & Δ Azimuth—30 degrees scan (Figure A-12)
         (d) Σ & Δ Azimuth—60 degrees scan (Figure A-13)
      (2) Patterns at 60 degrees per cycle scale
         (a) Σ Elevation (Figure A-14)
         (b) Σ & Δ Azimuth (Figure A-15)
   b. Patterns using rotating horn
      (1) Patterns using 360 degrees per cycle scale
         (a) Center Element—Azimuth (Figure A-16)
         (b) Σ Elevation (Figure A-17)

(c) Σ & Δ Azimuth (Figure A-18)

(d) Σ & Δ Azimuth–30 degrees scan (Figure A-19)

(e) Σ & Δ Azimuth–60 degrees scan (Figure A-20)

(2) Patterns using 60 degrees per cycle scale

(a) Σ Elevation (Figure A-21)

(b) Σ & Δ Azimuth (Figure A-22)

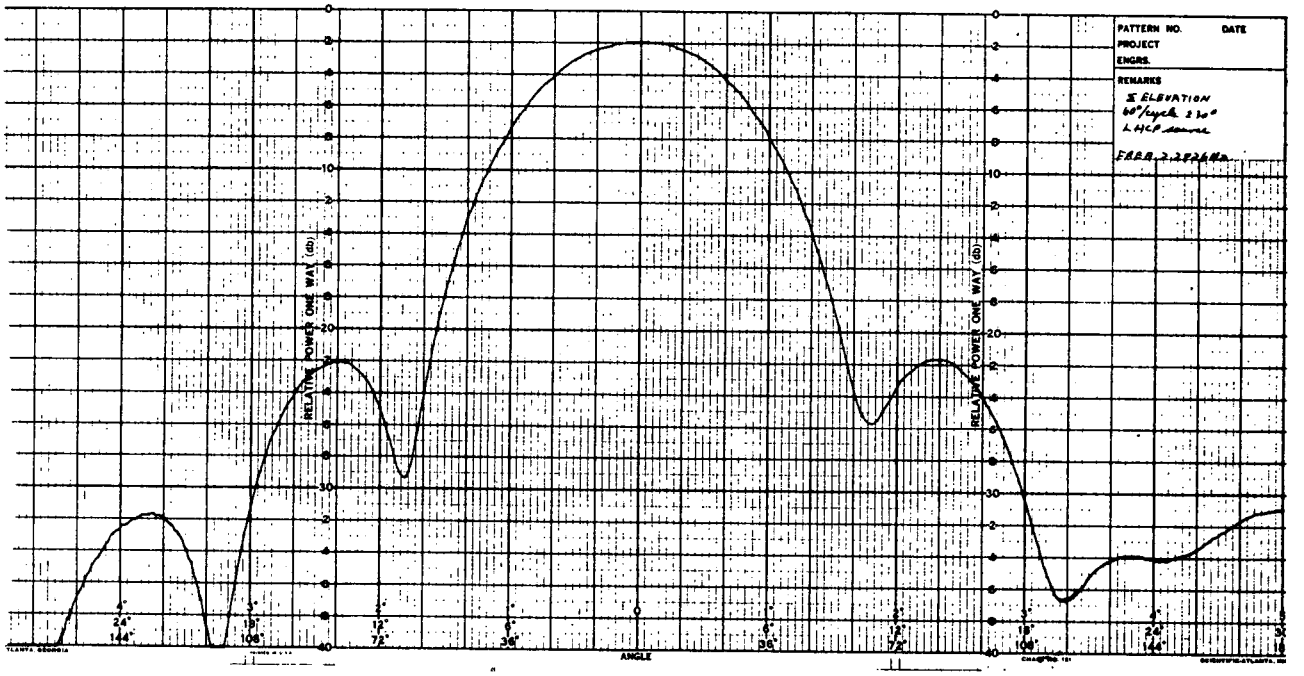

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Figure A-1. Σ Elevation, 60 Degrees per Cycle ±30 Degrees

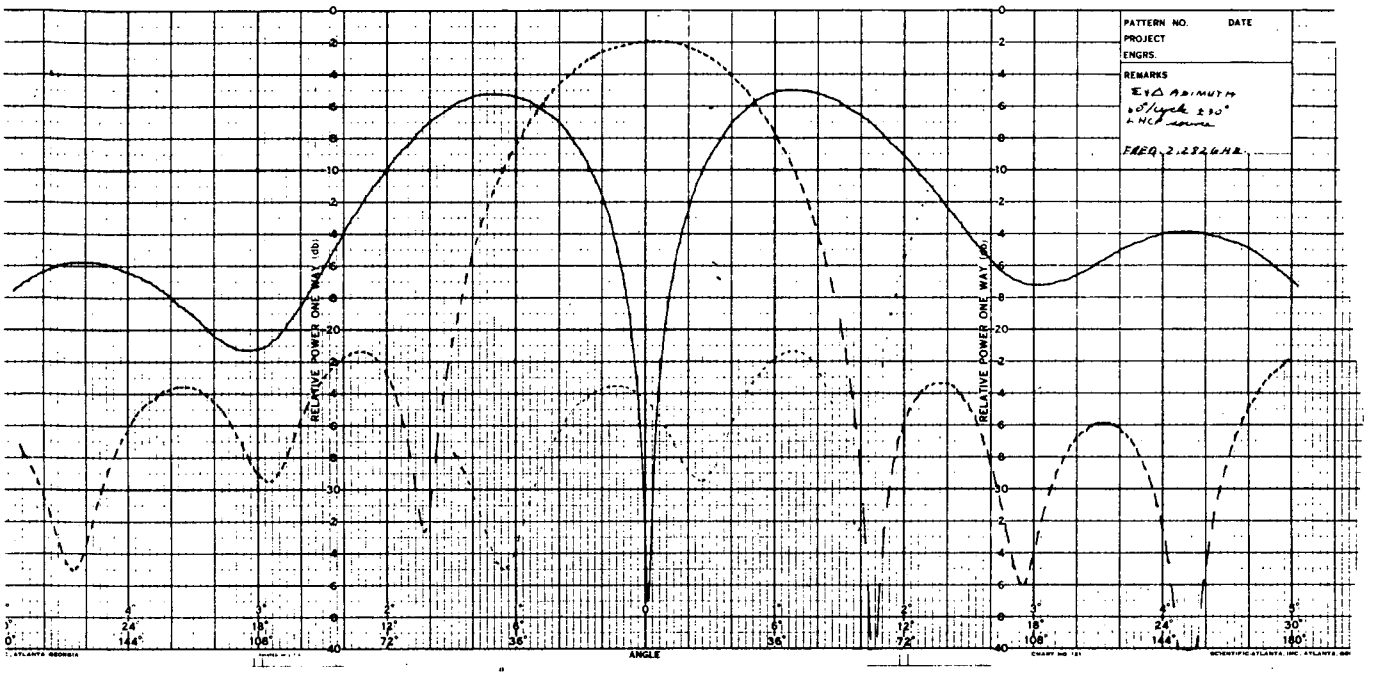

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Figure A-2. Σ and Δ Azimuth, 60 Degrees per Cycle ±30 Degrees

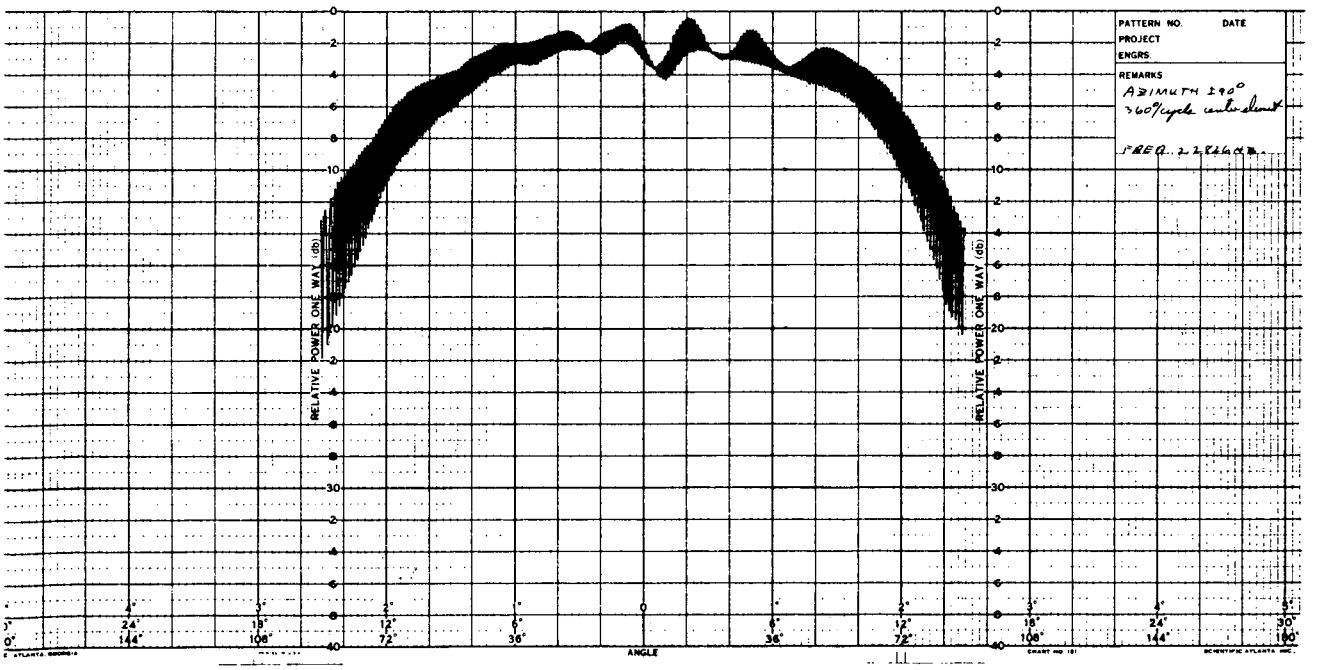

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Figure A-3. Azimuth ±90 Degrees, 360 Degrees per Cycle, Center Element

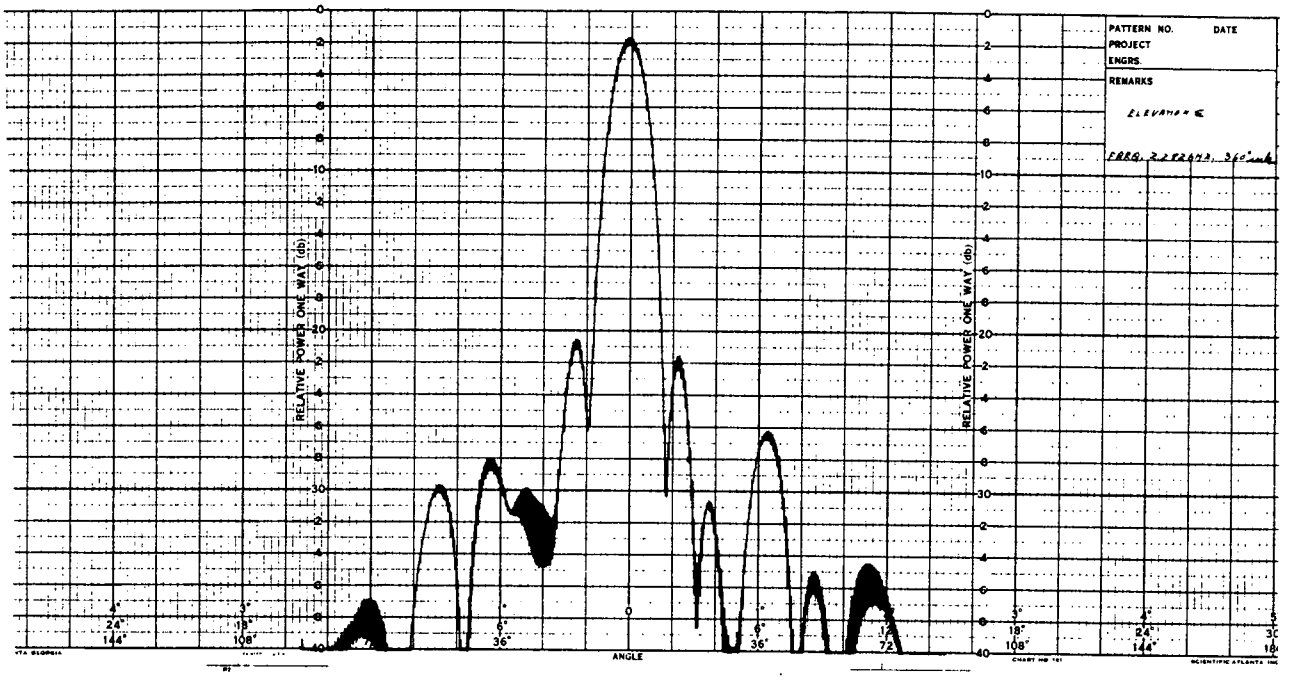

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Figure A-4. Σ Elevation, 360-Degree Scale

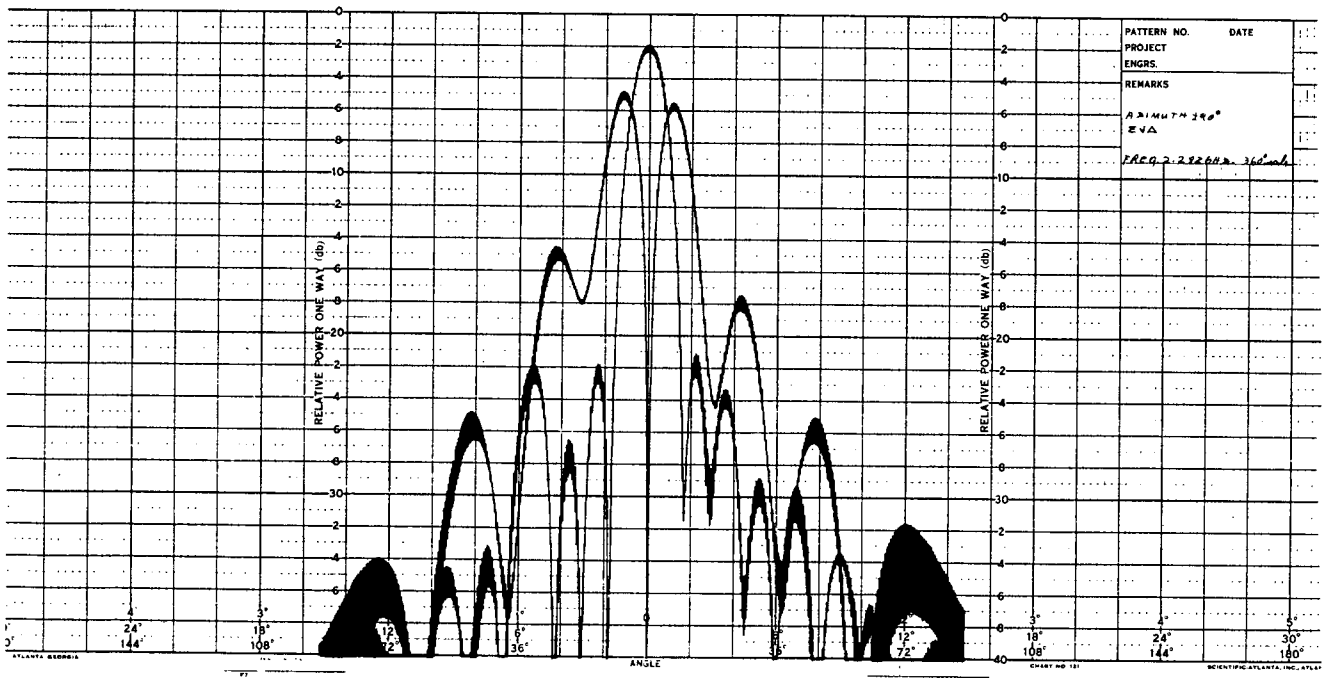

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Figure A-5. Σ and Δ Azimuth ±90 Degrees, 360-Degree Scale

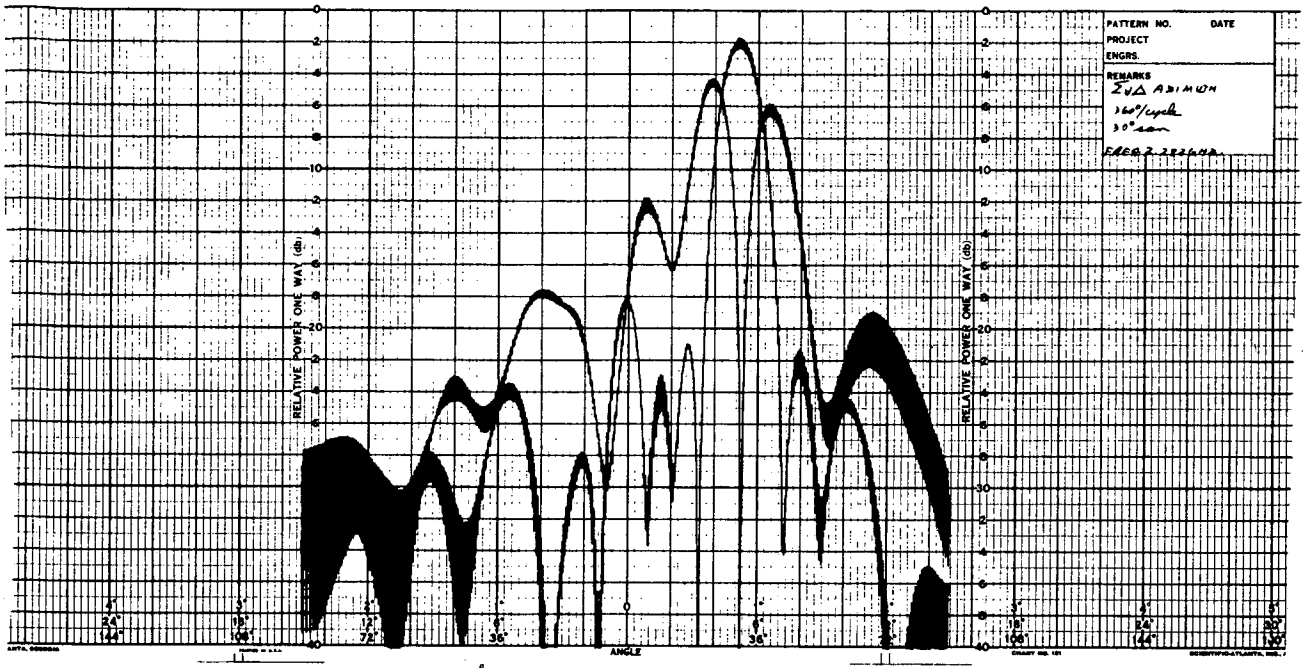

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Figure A-6. Σ and Δ Azimuth, 360-Degrees per Cycle, 30-Degree Scan

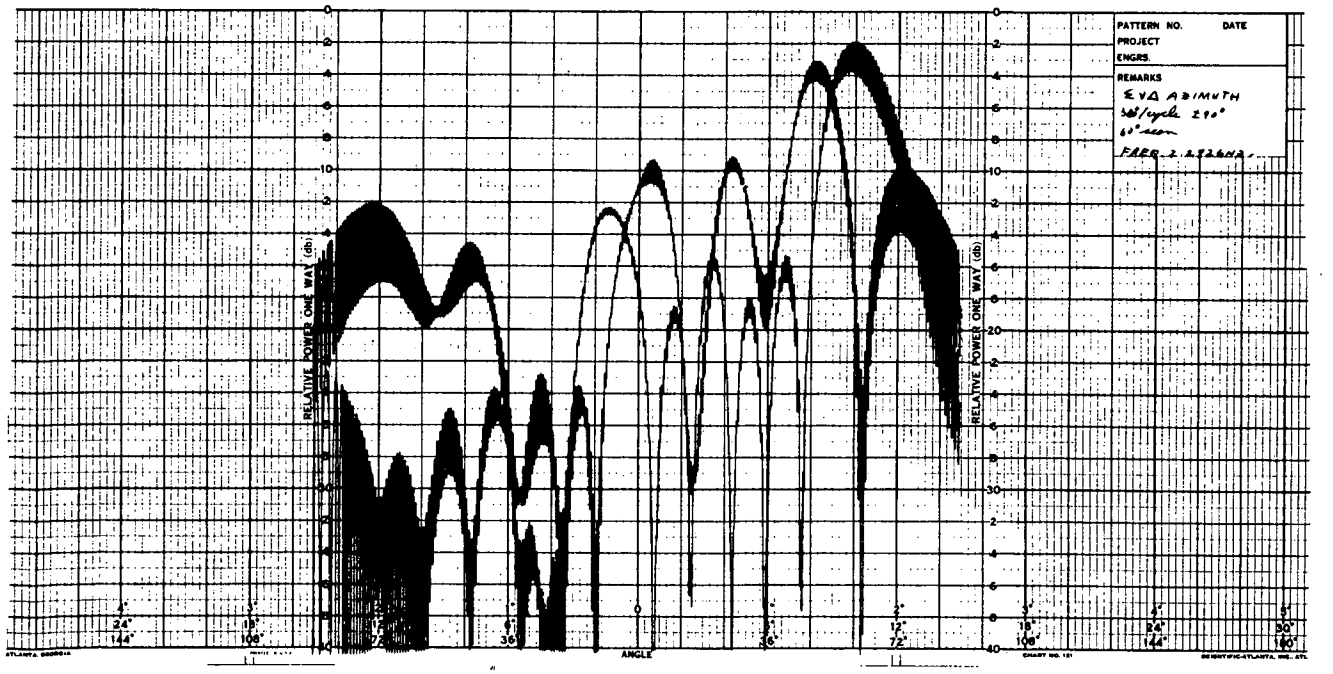

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Figure A-7. Σ and Δ Azimuth, 360 Degrees per Cycle ±90 Degrees, 60-Degree Scan

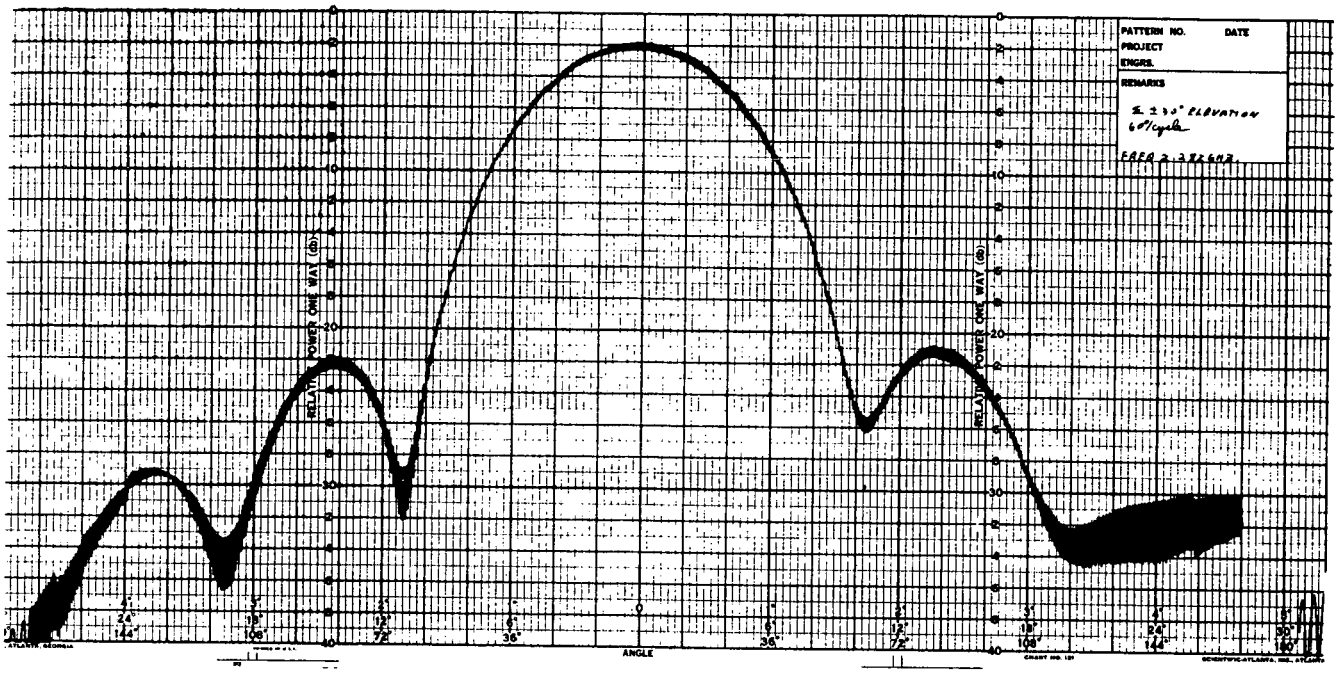

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Figure A-8. Σ Elevation ±30 Degrees, 60 Degrees per Cycle

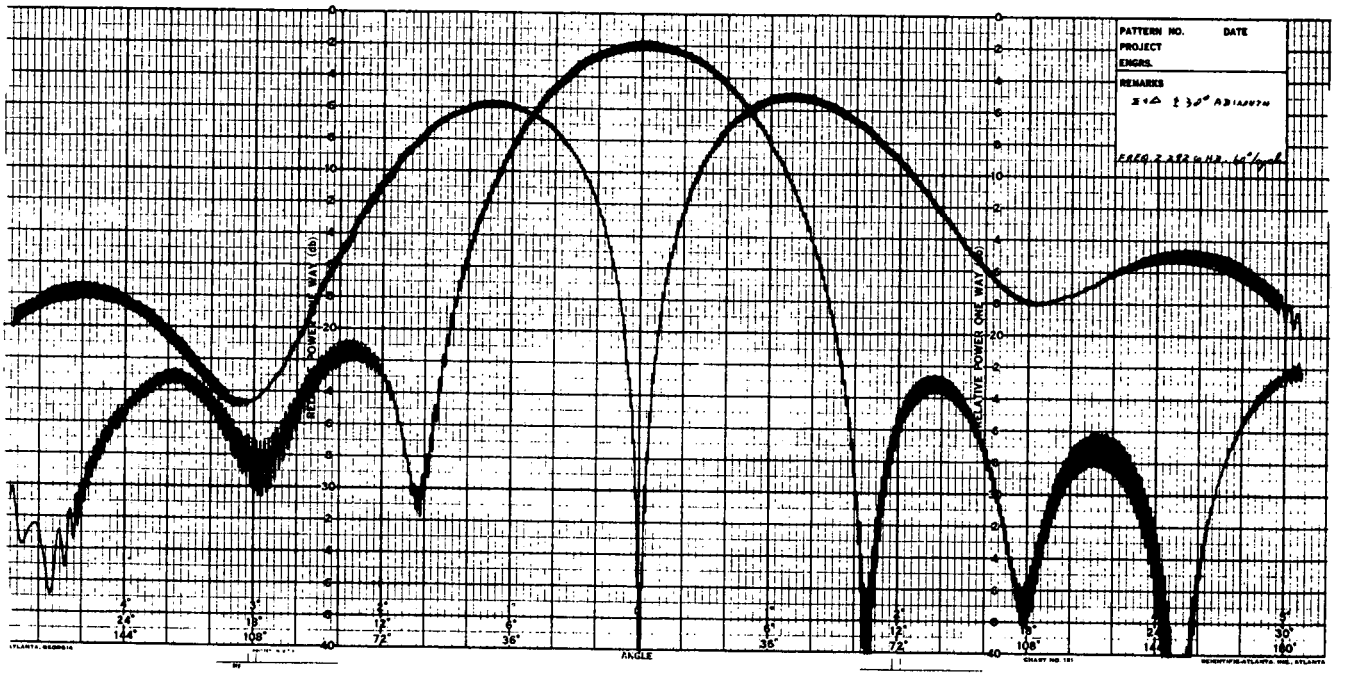

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Figure A-9. Σ and Δ Azimuth ±30 Degrees, 60 Degrees per Cycle

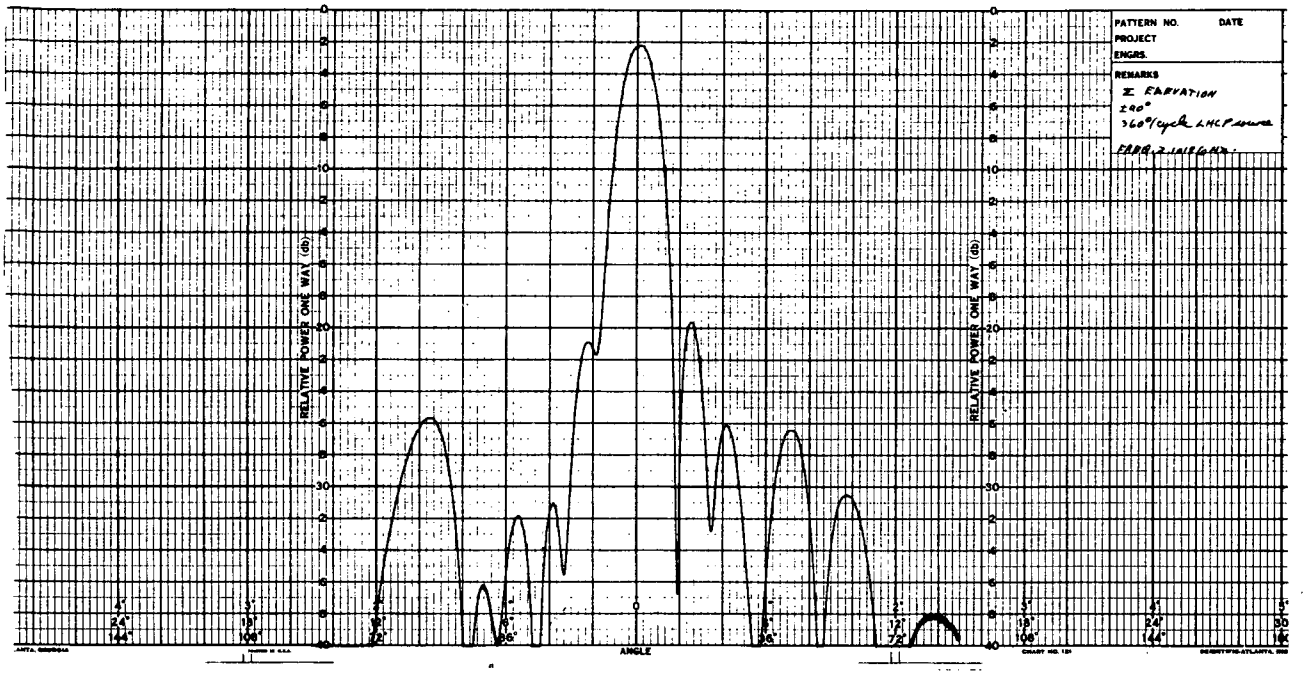

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Figure A-10. Σ Elevation ±90 Degrees, 360 Degrees per Cycle

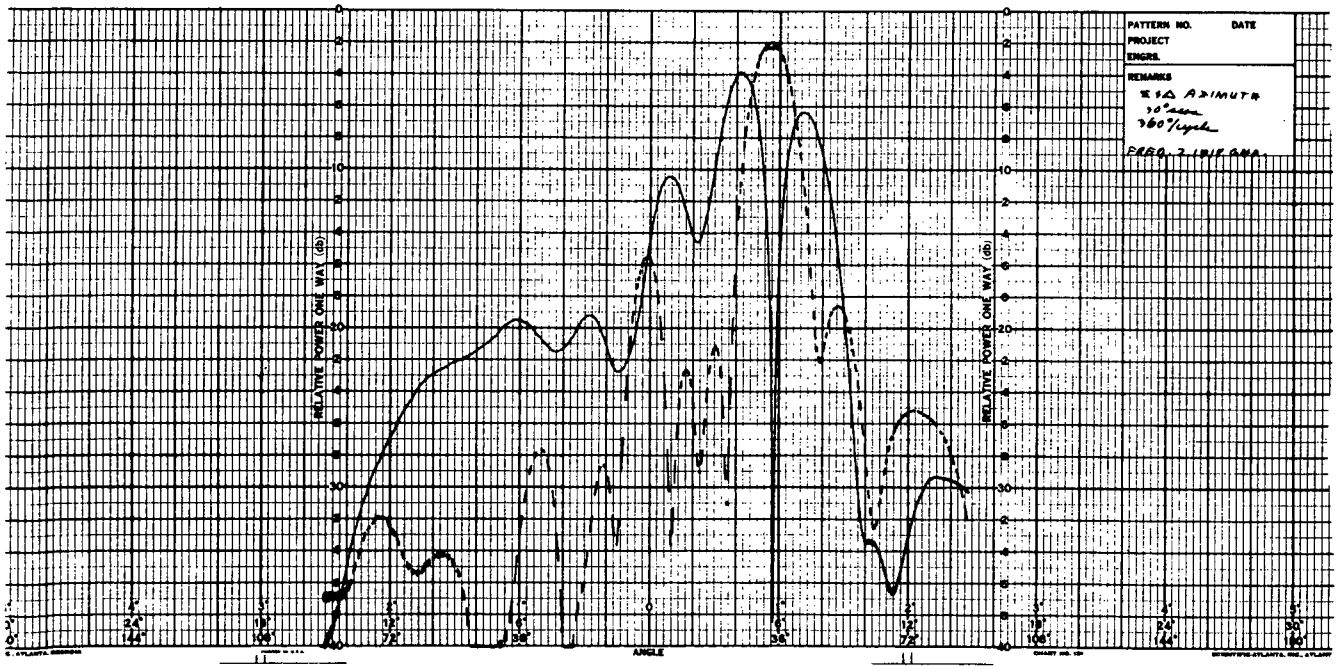

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Figure A-11. Σ and Δ Azimuth ±90 Degrees, 360 Degrees per Cycle

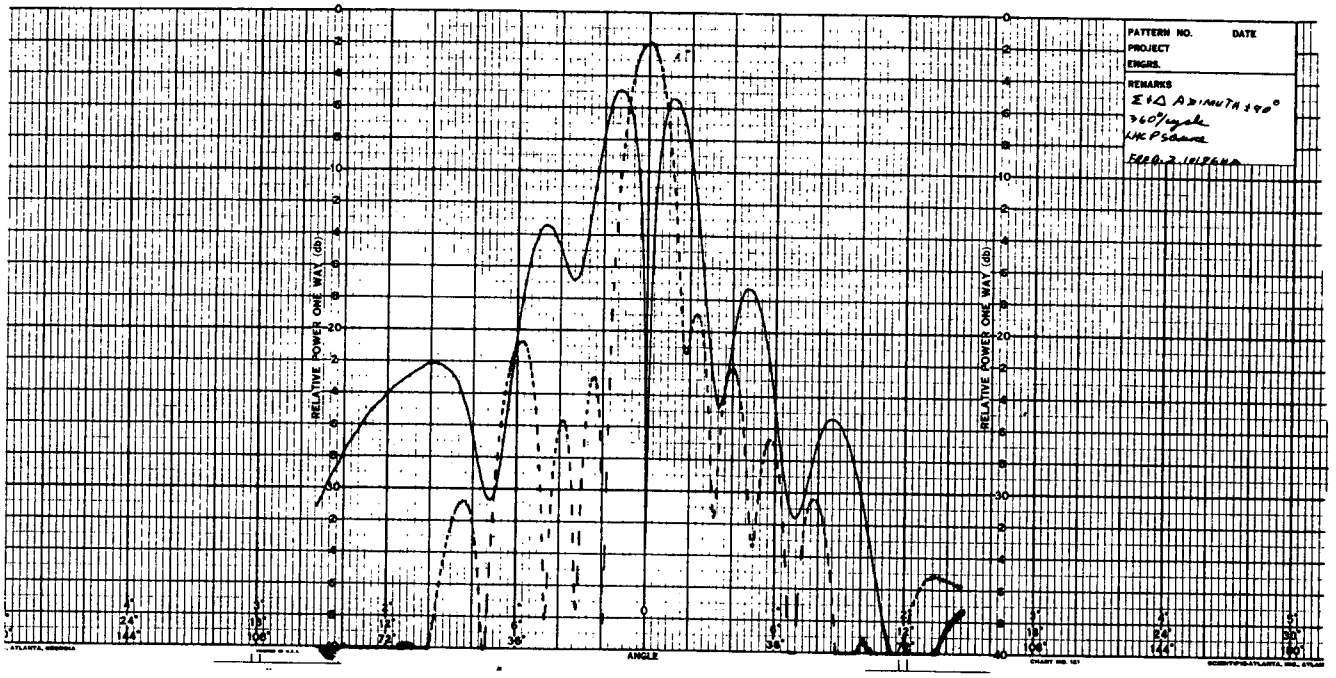

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Figure A-12. Σ and Δ Azimuth, 360 Degrees per Cycle, 30-Degree Scan

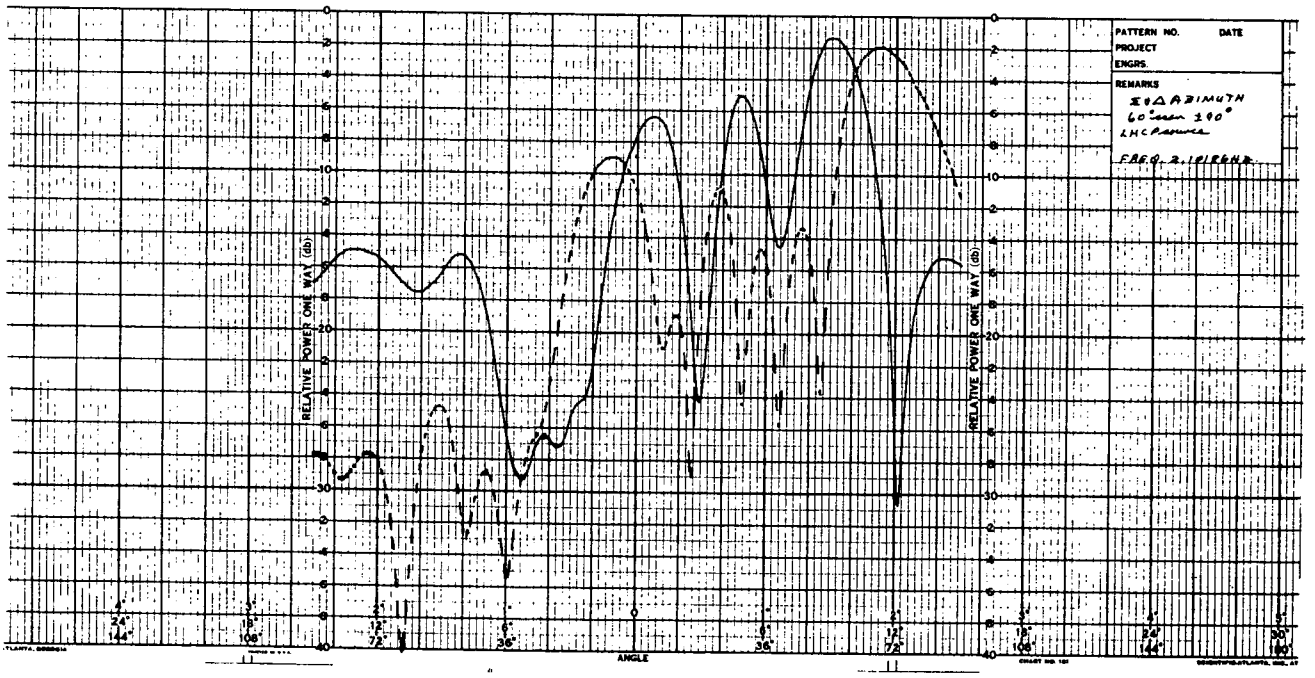

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Figure A-13. Σ and Δ Azimuth, 60-Degree Scan ±90 Degrees

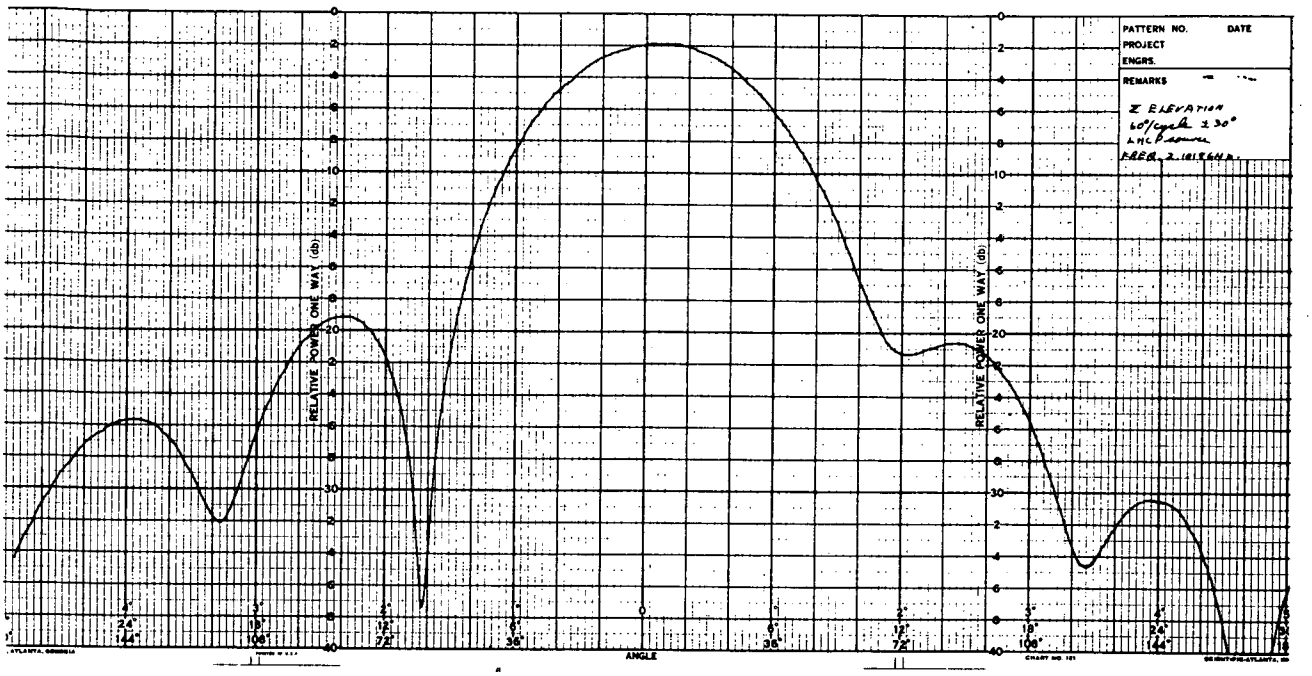

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Figure A-14. Σ Elevation, 60 Degrees per Cycle ±30 Degrees

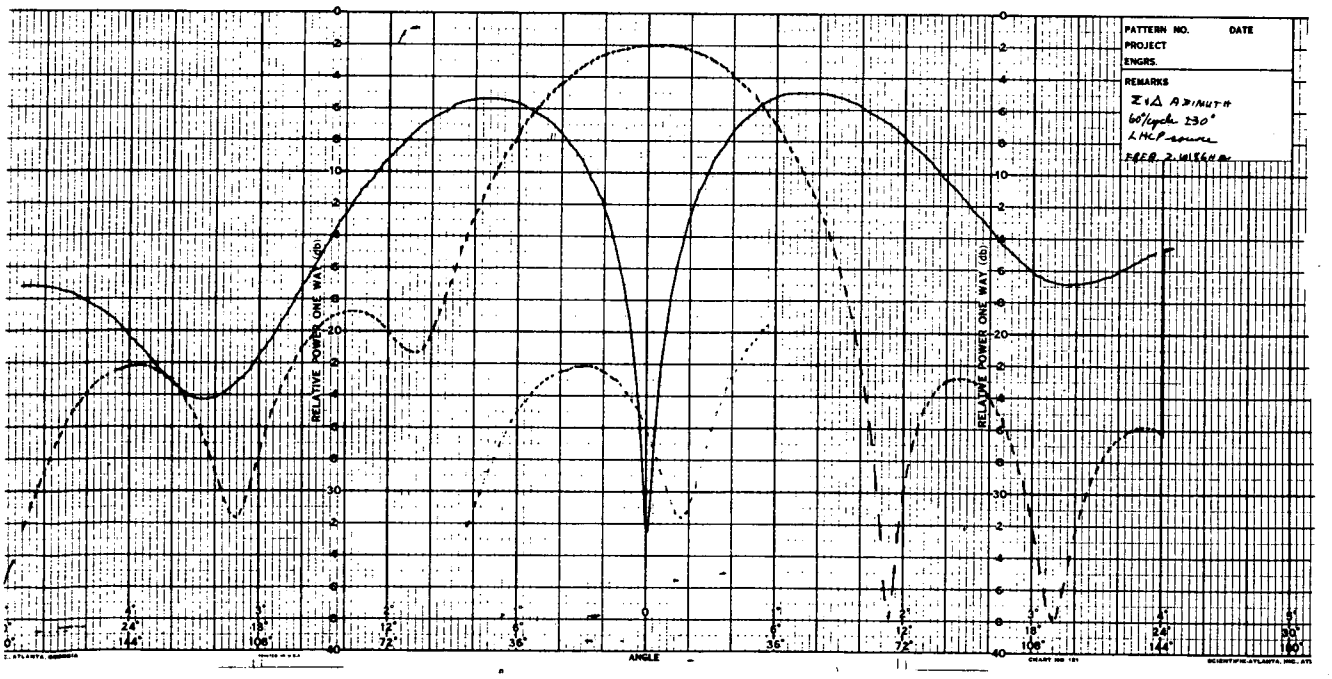

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Figure A-15. Σ and Δ Azimuth, 60 Degrees per Cycle ±30 Degrees

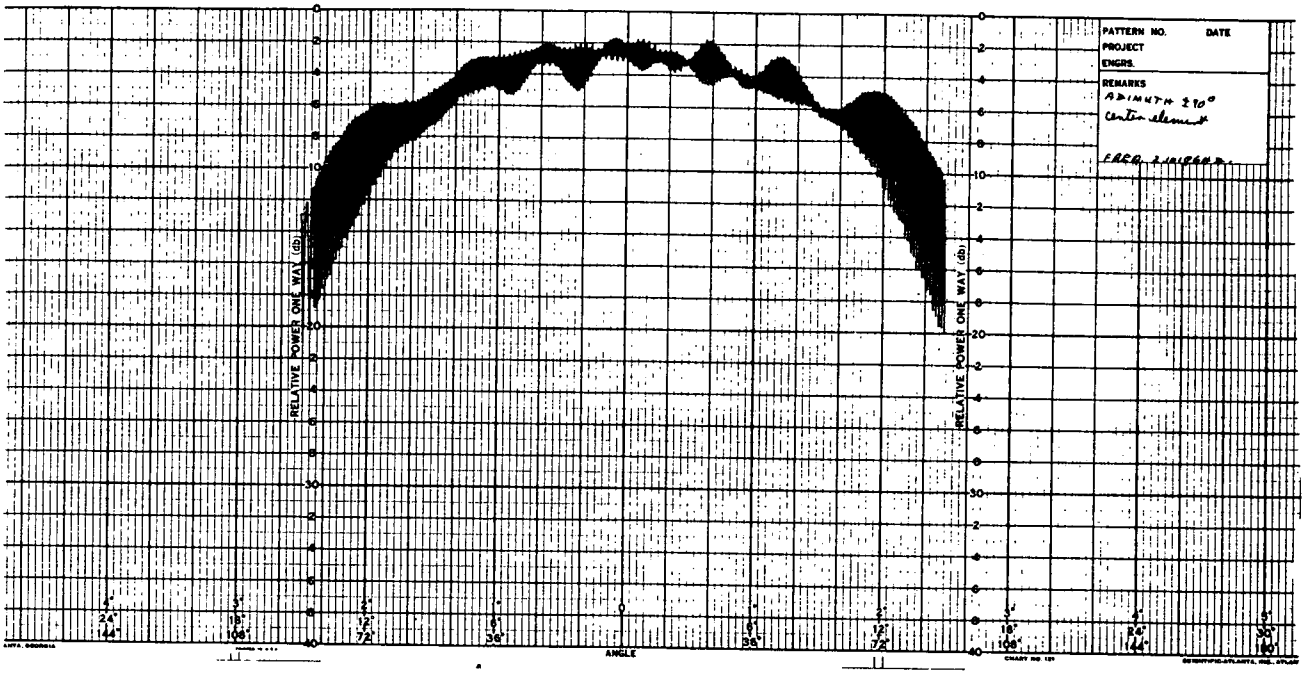

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Figure A-16. Azimuth ±90 Degrees, Center Element

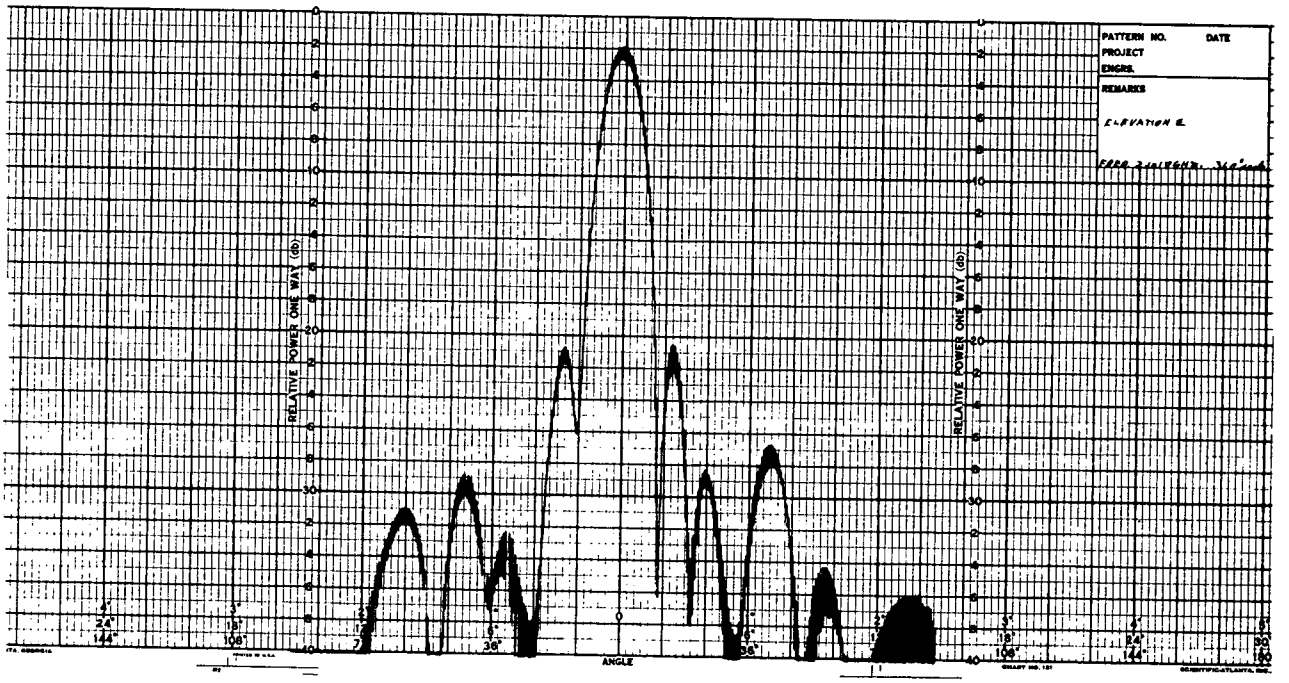

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Figure A-17. Σ Elevation, 360-Degree Scale

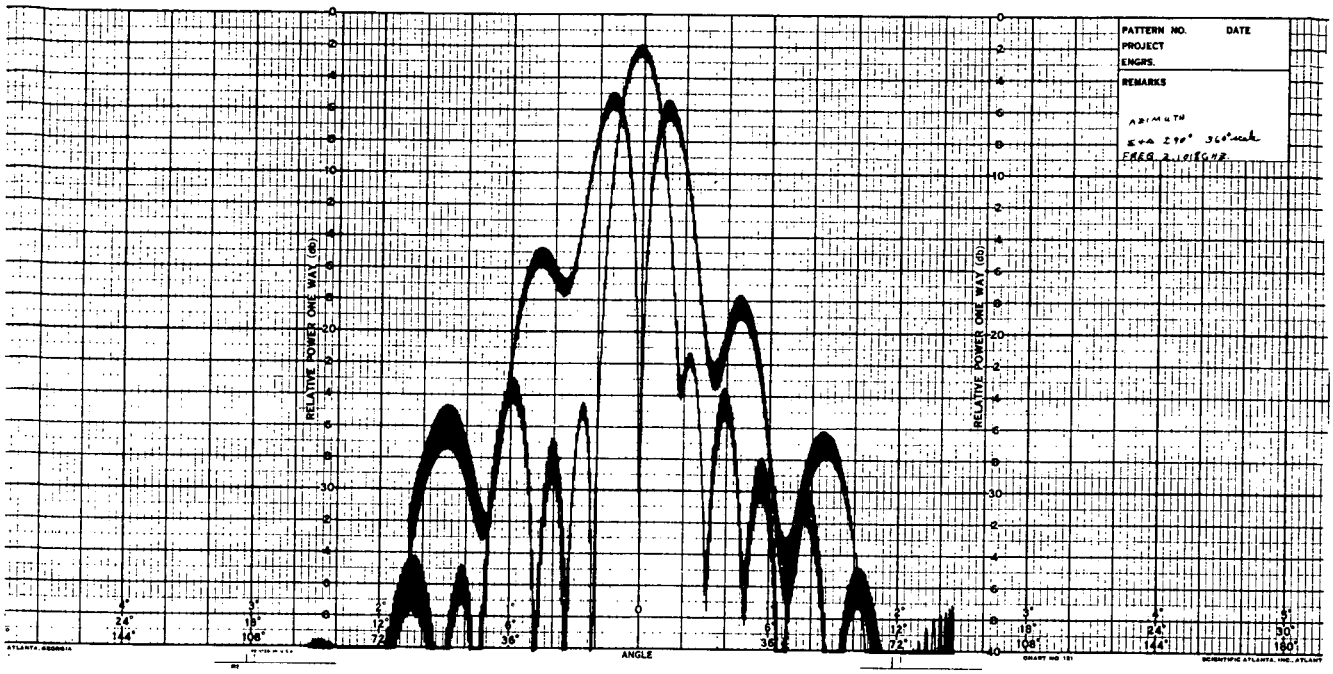

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Figure A-18. Σ and Δ Azimuth ±90 Degrees, 360-Degree Scale

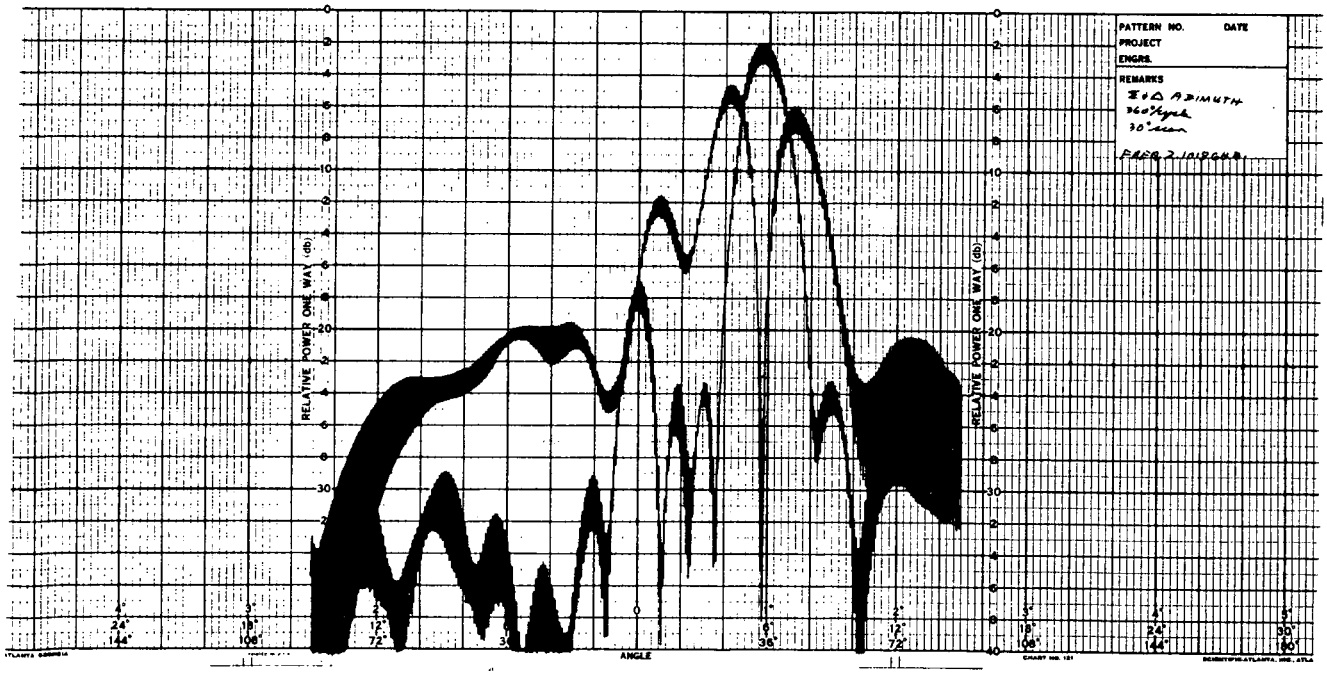

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Figure A-19. Σ and Δ Azimuth, 360 Degrees per Cycle, 30-Degree Scan

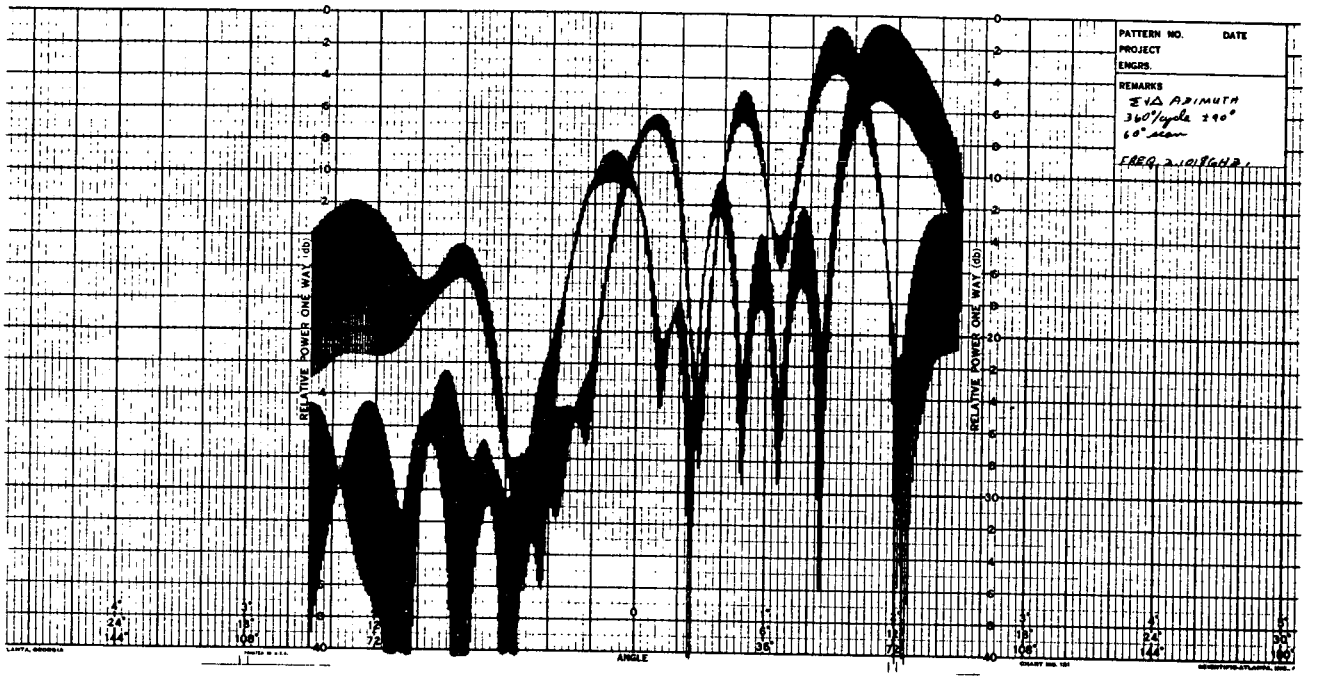

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Figure A-20. Σ and Δ Azimuth, 360 Degrees per Cycle ±90 Degrees, 60-Degree Scan

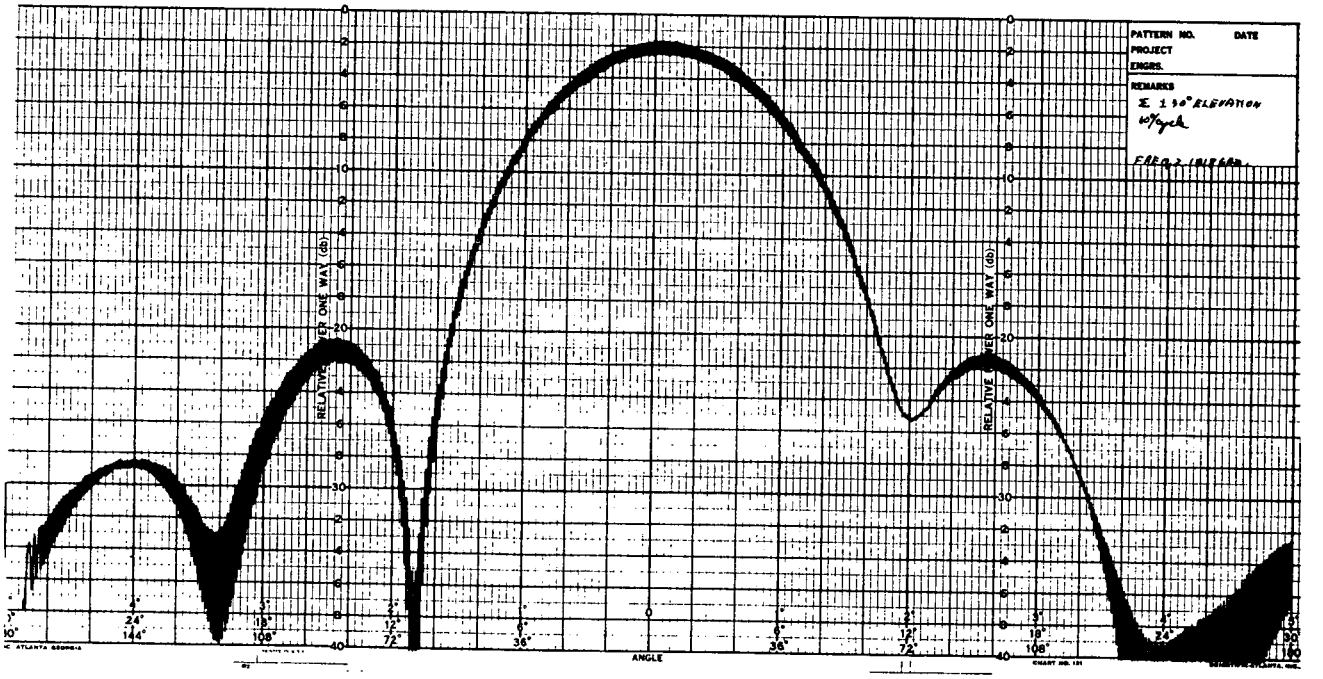

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Figure A-21. Σ Elevation ±30 Degrees, 60 Degrees per Cycle

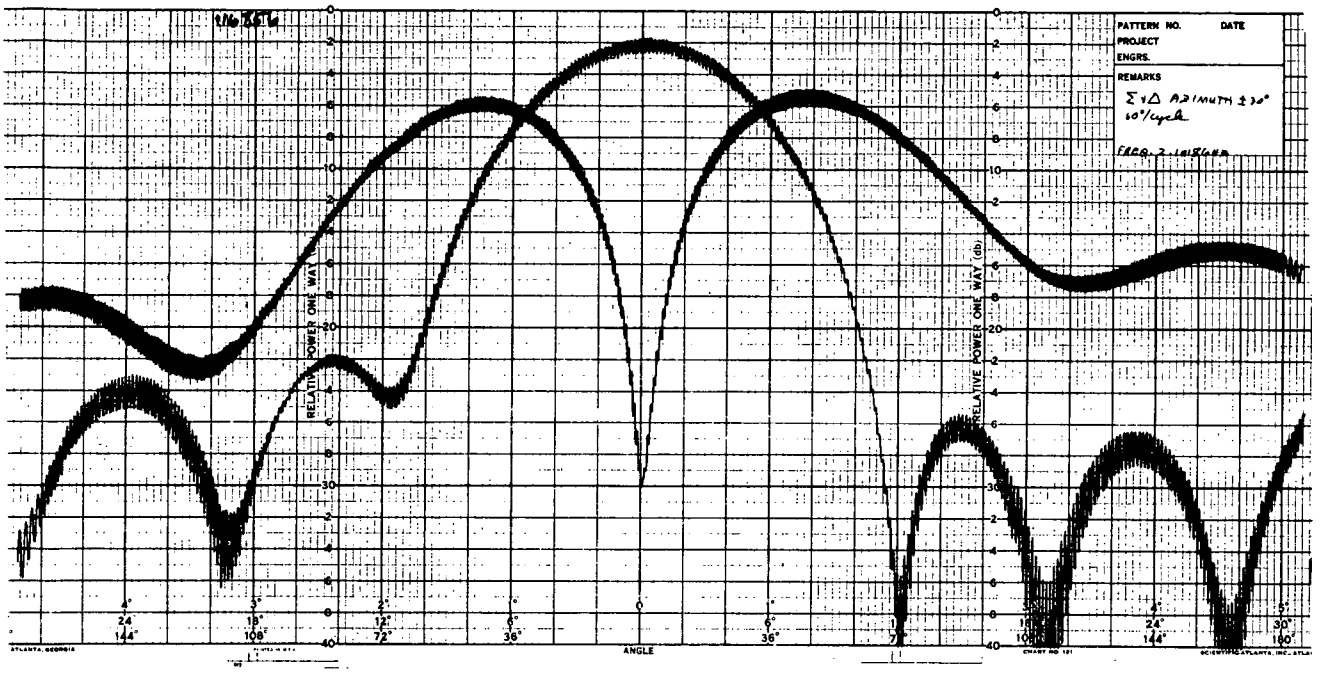

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Figure A-22. Σ and Δ Azimuth ±30 Degrees, 60 Degrees per Cycle

APPENDIX B
SUPPORTING DATA FOR RELIABILITY MODEL

Following are the failure rate breakdowns for each major block of the system.

A. Phased Array–RF Module

1. Transmit Channel

	Components	Quantity (η)	λ (per 10^6 hr)	$\eta\lambda$
Power Amplifier	Transistor (med power RF)	1	6.25	6.25
	Transistor (low power RF)	2	0.5	1.0
	Capacitor	8	0.03	0.24
	Resistor	6	0.01	0.06
	Bond	25	0.008	0.20
Phase Shifter	Capacitor	8	0.03	0.24
	Diode	10	0.05	0.50
	Bond	40	0.008	0.32
Logic	Integrated Circuit (digital)	4	0.08	0.32
	Resistor	8	0.01	0.08
	Bond	50	0.0008	0.40
Connector	Coax	2	0.02	0.04
	DC	6	0.015	0.09
	Circulator	1	0.1	0.10

$\lambda_t = 9.85$

2. Receive Channel

	Components	Quantity (η)	λ (per 10^6 hr)	$\eta\lambda$
Amplifier	Transistor (small signal)	3	0.05	0.15
	Capacitor	8	0.03	0.24
	Resistor	6	0.01	0.06
	Bond	27	0.008	0.216
Phase Shifter	Capacitor	8	0.03	0.24
	Diode (small signal)	10	0.05	0.50
	Bond	40	0.008	0.32
Logic	Integrated Circuit (digital)	4	0.08	0.32
	Resistor	8	0.01	0.08
	Bond	50	0.008	0.40
Connector	Coax	2	0.02	0.04
	DC	6	0.015	0.09
	Circulator	1	0.1	0.10

$\lambda_t = 2.756$

λ_e (phased array) = 1.7

B. Transmit Modulator

Components	Quantity (η)	λ (per 10^6 hr)	$\eta\lambda$
Transistor (small signal)	12	0.05	0.60
Diode (small signal)	12	0.05	0.60
Resistor	84	0.01	0.84
Capacitor	33	0.03	0.99
Integrated Circuit (linear)	8	0.15	1.20
Inductors	12	0.05	0.60
VCO	1	0.40	0.40
Bond	365	0.008	2.92
			$\lambda_t = 8.15$

C. Receiver

Component	Quantity (η)	λ (per 10^6 hr)	$\eta\lambda$
Transistor (small signal)	30	0.05	1.50
Resistor	114	0.01	1.14
Capacitor	100	0.03	3.00
Diode (PIN)	16	0.10	1.60
Inductor	58	0.05	2.90
Mixer (doubly balanced)	7	0.80	5.60
Oscillator (XTL)	1	0.40	0.40
Bond	750	0.008	6.00
			$\lambda_t = 22.14$

Redundancy with Repair $\lambda_e = 0.004$

D. Beam-Steering Computer

Integrated Circuit (digital)	55	0.08	4.40
Bonds	440	0.008	3.52
			$\lambda_t = 7.92$

E. Power Supply and Regulator

1. +28-Volt Supply and Regulator

Component	Quantity (η)	λ (per 10^6 hr)	$\eta\lambda$
Transistor (power)	3	0.35	1.05
Transistor (power)	1	0.40	0.40
Transistor (small signal)	1	0.05	0.05
Diode (power rect)	9	0.20	1.80
Diode (zener)	1	0.40	0.40
Diode (zener reference)	1	0.45	0.45
Transformer (power)	3	2.00	6.00
Capacitor (tantalum)	5	0.08	0.40
Capacitor (mica)	4	0.03	0.12
Resistor (metal film)	12	0.02	0.24
Inductors	3	0.05	0.15
Integrated Circuit (linear)	1	0.15	0.15
Bonds	150	0.008	1.20
			λ_t = 12.41
		2 required	x 2
			λ_t = 24.82

2. +5-Volt Supply and Regulator

Slightly less complex than the +28-volt regulator $d_t = 12.20$

3. +12-, +1.3-, and ±12-Volt Supply and Regulator

Component	Quantity (η)	λ (per 10^6 hr)	$\eta\lambda$
Transistor (power)	3	0.35	1.05
Transistor (power)	1	0.40	0.40
Transistor (small signal)	1	0.05	0.05
Diode (power rect)	18	0.20	3.60
Diode (zener)	1	0.40	0.40
Diode (zener reference)	1	0.45	0.45
Transformer (power)	3	2.00	6.00
Capacitor (tantalum)	7	0.08	0.56
Capacitor (mica)	4	0.03	0.12
Resistor (metal film)	14	0.02	0.28
Inductors	4	0.05	0.20
Integrated Circuit (linear)	1	0.15	0.15
Bonds	175	0.008	1.40
		Power Supply and Regulator λ_t =	14.66
		Total λ_t =	51.68

Redundancy with Repair[33] λ_e = 0.004